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Design Notice – RT5081

History

Revision	Date	Author	Description
V0.1	2016/11/10	Jacky	Initial
V0.2	2016/11/11	Jacky	1.Modify CFO_EN and CHG_EN description 2.Add Power Path Circuit Design description 3.Modify AICR description 4.Modify BL PWM resolution select description 5.Modify RGB Breath mode description
V0.3	2016/12/14	Jacky	1.Modify C1 & C2 voltage rating 2.Modify PD_VCONN5V circuit 3.Modify BAT_COMP range 4.Modify ADC channels table 5.Modify strobe mode current range 6.Add VBAT operation range to avoid trigger BL OCP 7.Update Normal #1 LDO Layout Constraints 8.Add diode P/N suggestion between PD_VCONN5V and VSYS 9.Add Minimum PCB placement area requirement 10.Modify OVP controller description 11. Add Apple TA Detection solution
V0.4	2016/12/29	Jacky	1.Add Note of BL recommend operation range for heavy load 2.Add OVP Controller Specification 3.Add TVS selection Guide for Surge Protection
V0.5	2017/1/3	Jacky	1.Modify BL recommend operation range for heavy load

History

Revision	Date	Author	Description
V0.6	2017/01/09	Yan	1.Modify C1 & C2 voltage rating 2.Maximum inductor current calculation in Back-light. 3.Maximum inductor current calculation in Display bias.
V0.7	2017/01/24	Jacky	1.Modify ADC formula description
V0.8	2017/03/07	Jacky	1.Add note of turn-on/off sequence of BL and DB 2.Add note of BL mode change
V0.9	2017/03/31	Jacky	1.Add OVP type comparison 2.Add TVS for VBAT surge protection

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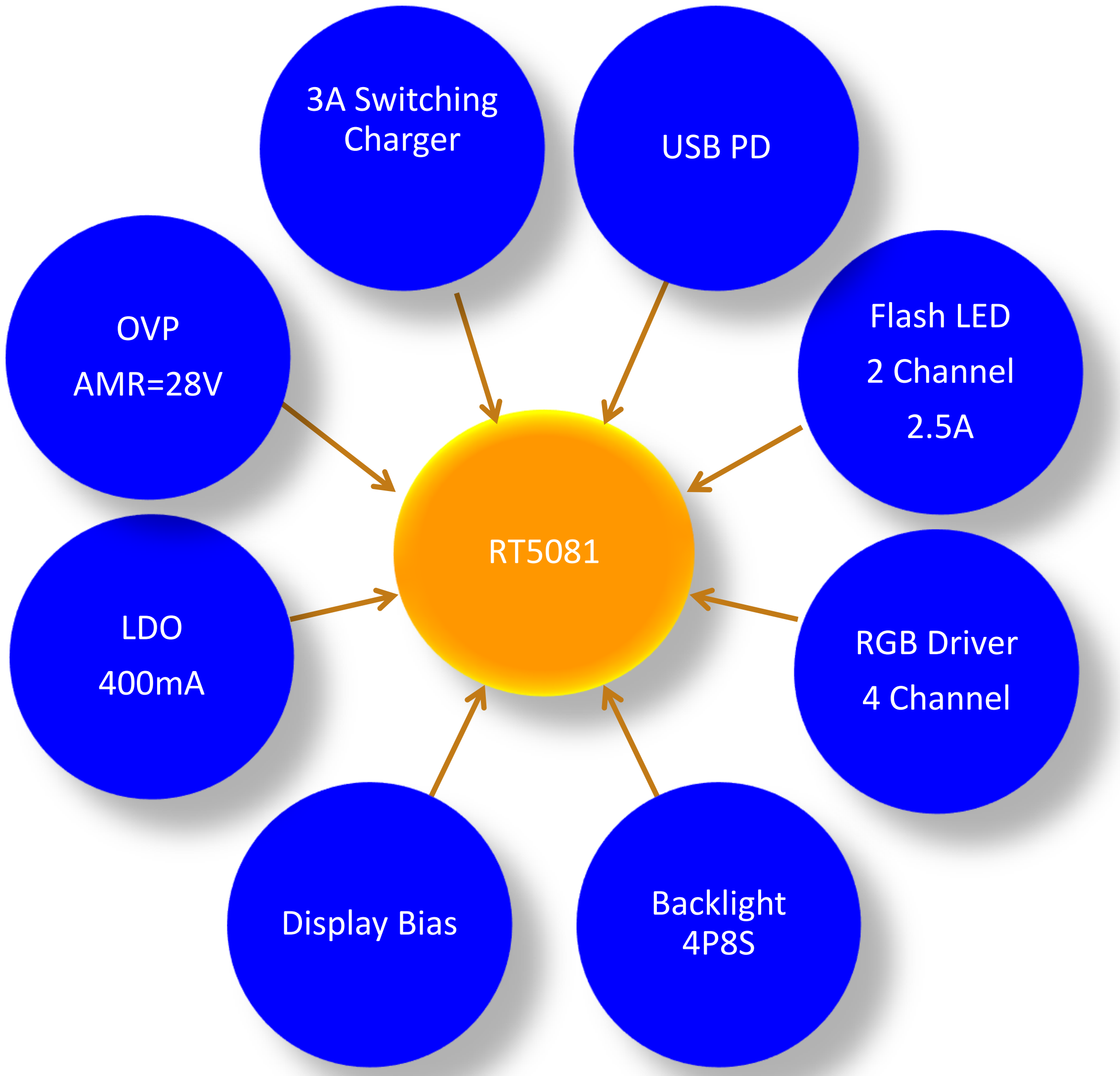
- General Function Description
- Component Selection Guide
- Schematic/Layout Notice

Block Interface Overview



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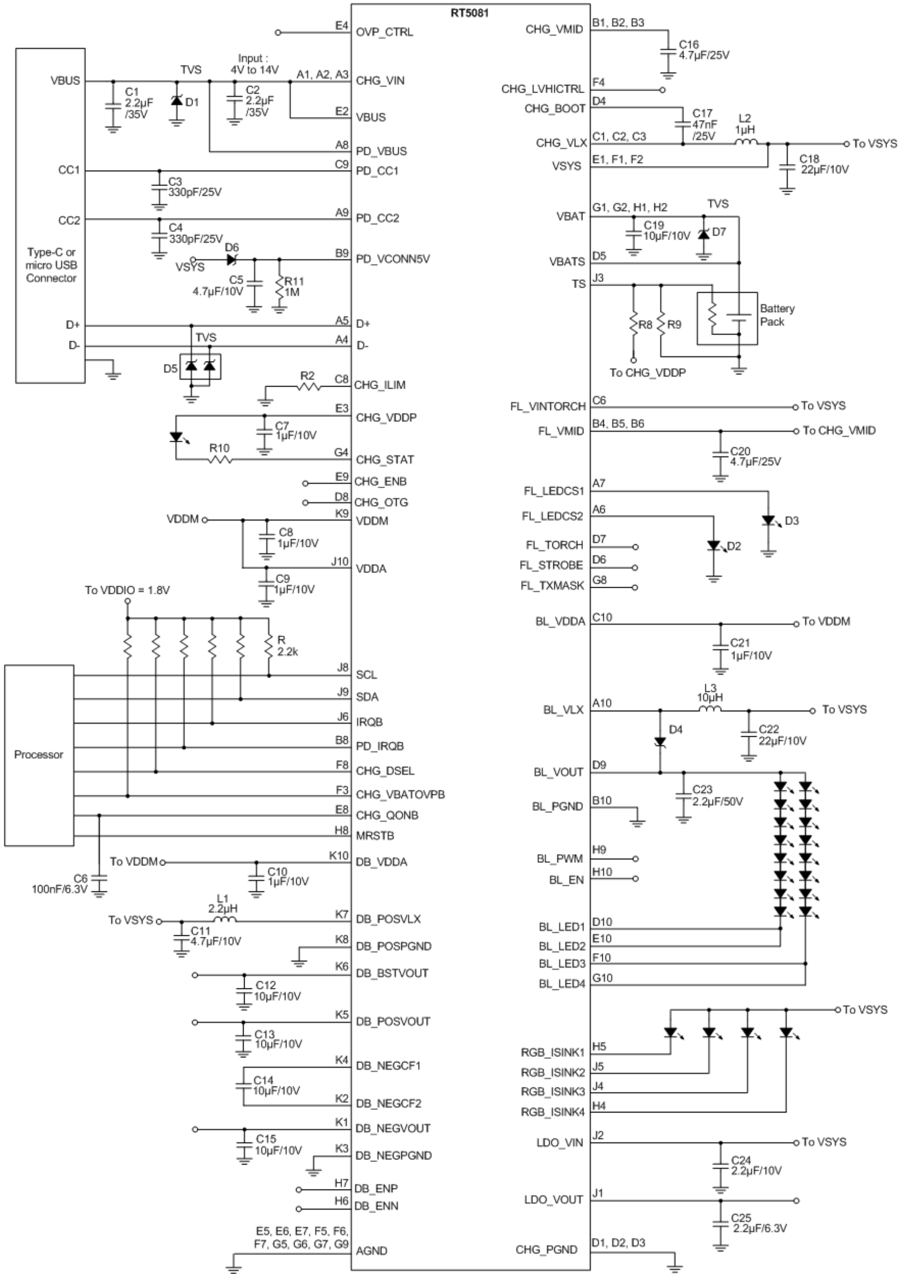
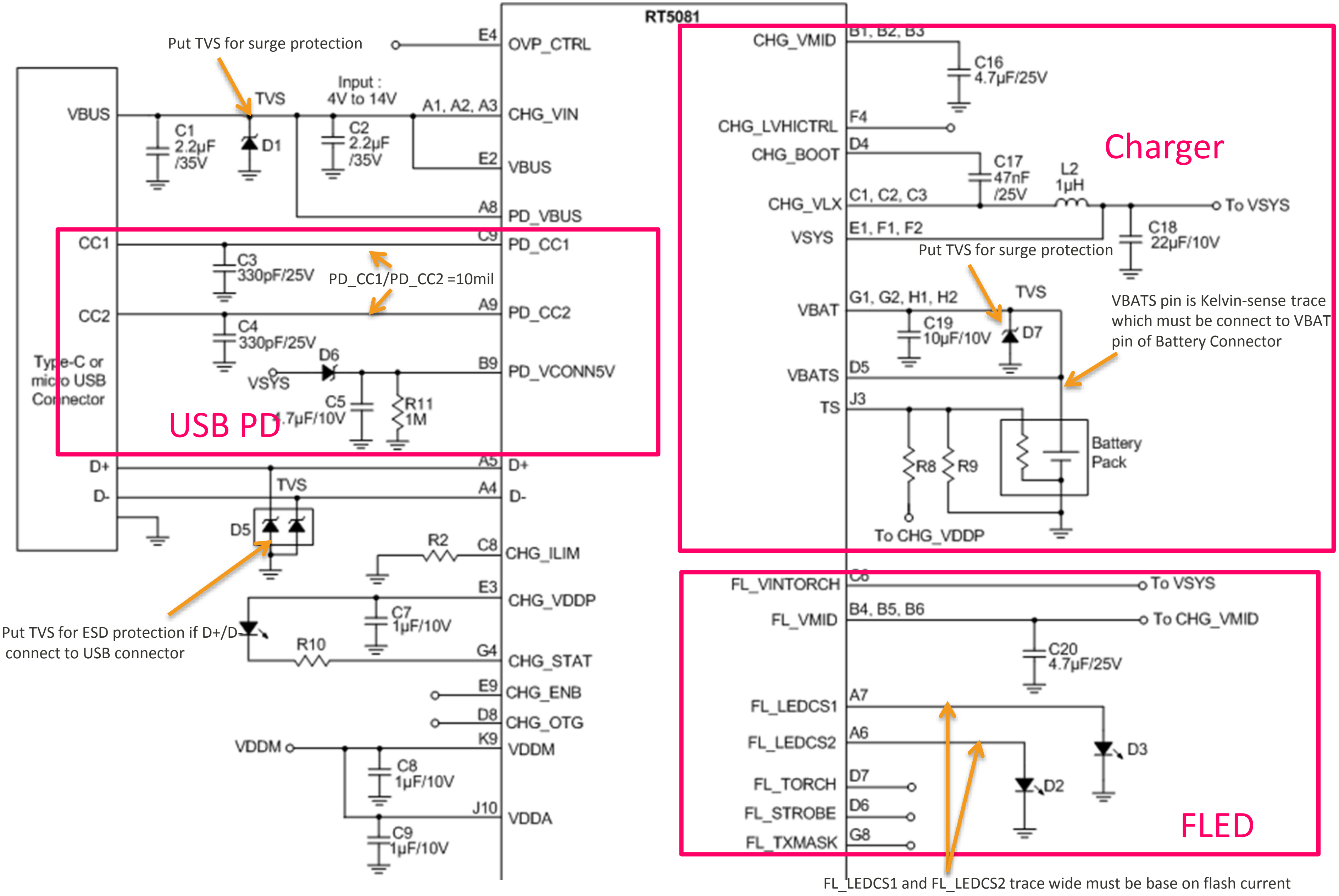
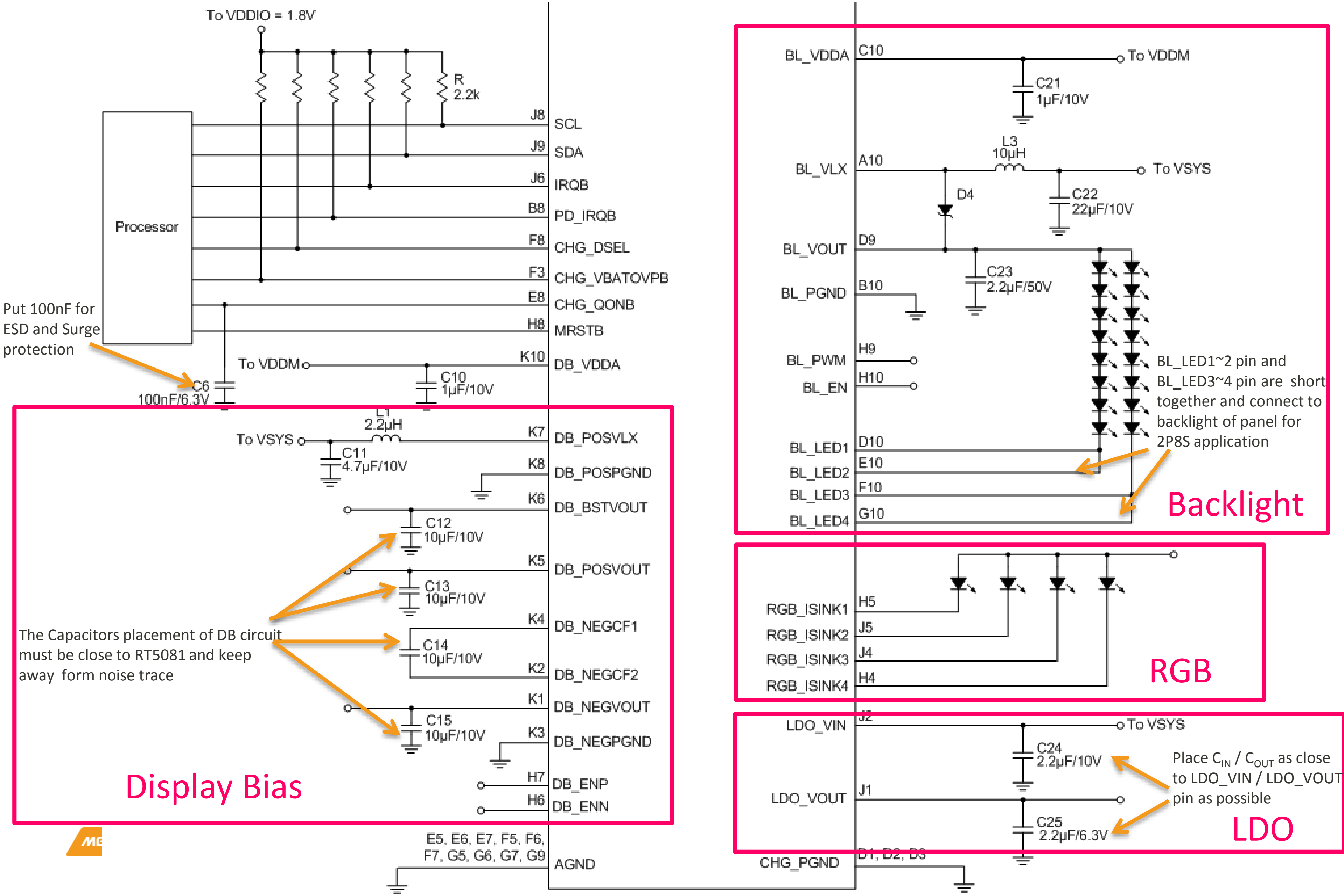
Schematic Overview



Schematic Overview



Schematic Overview



Charger Feature list

Feature list	Description
Charge Current Regulation	ICC level: 0.1A/0.2A~5A, 0.1A/step
	VBAT = 3.8V, ICHG > 1000mA(TC = 30°C to 65°C), Accuracy ±7%
Charge Voltage Regulation	CV level: 3.90V/3.91V~4.71V, 10mV/step
	VOREG_CHG = 4.2V or VOREG_CHG =4.34V (TC = 0°C to 85°C, ±1%) (TC =25°C, ±30mV), Accuracy ±1%
Average Input Current Regulation (AICR)	AICR level: 0.1A/0.15A~3.25A, 50mA/step
Synchronous 1.5Mz/0.75MHz Fixed-Frequency PWM	Default: 1.5MHz 0.75MHz / 1.5MHz selectable
	Controller with up to 95% Duty Cycle
Thermal Regulation and Protection	Default: 120℃ 60 ℃/ 80 ℃ / 100 ℃/120 ℃ selectable
Over-Temperature Protection	Thermal shutdown threshold temperature = 160℃, Hysteresis=20℃
Input Over-Voltage Protection	With external OVP Controller: 16.5V
	Without external OVP Controller: 14.5V
USB OTG	Default: 5.05V OTG output voltage range:4.425V~5.825V, 50mV/step
	Default: 0.5A OTG OC: 0.5A/0.7A/1.1A/1.3A/1.8A/ 2.1A/2.4A/3A
BC1.2 charger detection	BC1.2 charging port compliance
Integrated ADCs for System Monitoring	ADC channel: VBUS_DIV5/VBUS_DIV2/VBAT/VSYS/CHG_VDDP/TS_BAT/IBUS/IBAT/TEMP_JC
HW JEITA	Japan JEITA compliance, HW auto charging regulation to protect battery under extremely High/low temp. condition
Low Battery Protection for Boost Operation	Default :2.8V 2.8V/2.9V~3.8V, 0.1V/step
Charging Watchdog (reset to default)	Watchdog time-out protection to stop charging
Charging Safety timer	
IRQ (interrupt function)	IRQ pin support INT to AP
CHG_STAT	1. Support I^2C control ON/OFF state 2. Charging indicator
PE+1.1 / PE+ 2.0	Support MTK PumpExpress Plus 1.1 and 2.0 by HW auto-control sink current pattern

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Flash LED Driver Feature list

Feature list	Description
Synchronous Boost Dual Flash LED Driver with Dual Independently-Programmable LED Current Sources	The max strobe current of each channel = 1.5A
	The total max strobe current of 2 channels = 2.5A
I^{2}C-Programmable Flash Safety Timer	FLED strobe timeout: 64ms/96ms~2432ms, 32ms/step
Flash LED1/LED2 Short-Circuit Protection, and Output Short-Circuit Protection	LEDCS Short protection threshold < 1V, delay time = 2.5ms
TX Mask Protection with dedicated FL_TXMASK Pin	Default: TX_ActiveLevel=H TX_ActiveLevel=L / TX_ActiveLevel=H selectable
	Default: ALL FLEDs' TX function disable Can select only LEDCS1 or LEDCS2 or both LEDCS1 & LEDCS2 be enabled TXMASK function
Shared Charger/OTG as Power Stage	Can save one inductor cost by use the same boost circuit of OTG mode
Support Auto-Tracking Mode	Default: Fix mode MID Regulation Level by Fix mode/MID Regulation Level by auto-tracking selectable
	Can gain more efficiency by Auto-Tracking Mode
Independent Torch Bypass MOSFET from VSYS	TA can also support Torch current
Torch Mode Current	Torch mode current level: 25mA/37.5mA~400mA, 12.5mA/step
Strobe Mode Current	ULTRA LOW ISTRB=0 Strobe mode current level: 50mA/62.5mA~1500mA, 12.5mA/step
	ULTRA LOW ISTRB=1 Strobe mode current level: 25mA/31.25mA~750mA, 6.25mA/step

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Backlight WLED Feature list

Feature list	Description
Drives up to 8 series WLEDs in 4 Strings	Each channel can source up to 30mA
Dimming by external PWM Pin and I^2C-Controlled with Programmable 11 bits	Linear and Exponential mode Brightness control
I^2C-Programmable Over-Voltage Protection (OVP) Threshold	Default: 29V 17V/21V/25V/29V selectable
Supports Torch Mode and Strobe Mode for Front Cameras	**Front-Facing Flash with 300% Brightness for selfie shot**
Auto Switch Frequency Mode	< Auto Frequency select (register 0xA6[7:0]), 500kHz
	>Auto Frequency select (register 0xA6[7:0]), 1MHz
Four Over-Current Protection Thresholds	Default: 1500mA 900mA/1200mA/1500mA/1800mA selectable

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Display Bias Feature list

Feature list	Description
Flexible Output Voltages (VBST, VPOS, VNEG) Setting	I^2C-Programmable Output Voltages
Boost Converter Output Voltage (VBST) Range	Default :5.7V 4V/4.05V~6.2V, 50mV/step
Positive Voltage Output (VPOS) Range	Default :5.5V 4V/4.05V~6V, 50mV/step
Negative Voltage Output (VNEG) Range	Default :-5.5V -4V/-4.05V~-6V, 50mV/step
Positive/Negative Voltage can be selectable Output Mode	Fast Discharge or Float
External Independent Positive/Negative Enable Control	VPOS/ VNEG can be controlled by separate or together
BST Current Limit	≥ 1.1A, Cycle by cycle detection. If OCP occurs, LG off
POS Short-Circuit Protection	$VPOS \leq 0.8 \times VPOS_{(Target)}$
NEG Short-Circuit Protection	$VNEG \leq 0.25 - 0.8 \times (-VNEG_{(Target)})$
Output Current ability	50mA
Power-Saving by Periodic Mode	Default: 20Hz 20Hz / 33Hz selectable

RGB Feature list

Feature list	Description
4-Channel LED Driver	RGB_ISINK1~4 can support Register mode, PWM mode and Breath mode
	RGB_ISINK4 for CHG_VIN Power Good Indicator
	Default: RGB_ISINK4 is AUTO mode(Charger Indicator) AUTO mode(Charger Indicator)/ Software mode selectable
Sink Current for 3 RGB LEDs	Default :8mA 4mA/8mA~24mA, 4mA/step
PWM Dimming Frequency	Default :0.2Hz PWM Frequency: 0.1Hz/0.2Hz/0.5Hz/1Hz/2Hz/5Hz/200Hz/1KHz
Breath Mode	Programmable breathe mode by set Tr1, Tr2, Tf1, Tf2, TON, TOFF parameters

LDO Feature list

Feature list	Description
Wide Operating Voltage Range	LDO_VIN range: 1.8V to 5V
Wide Operating Voltage Ranges	Default: 3.4V LDO_VOUT: 1.6V/1.8V~4V, 0.2V/step
Output Current	400mA
Low Dropout Voltage	180mV at 300mA
High PSRR	50dB at the below conditions: VINL = 3.6V, VOUT = 2.8V, IOUT = 20mA@1kHz, LDO_COUT = 2.2uF
Current Limit Protection	600mA

USB PD Feature list

<table>
<tr><th>Feature list</th><th>Description</th></tr>
<tr><td rowspan="2">USB PD Power role Support</td><td>Dual-role PD compatible</td></tr>
<tr><td>Attach/Detach detection as host, device or DRP</td></tr>
<tr><td rowspan="2">Current capability definition and detection</td><td>OTG mode:
Vlotage:5V+/-5%
Current:3A max</td></tr>
<tr><td>Sink mode:
Vlotage:5V~14V+/-5%
Current:3A max</td></tr>
<tr><td>Cable recognition</td><td>Get e-marked cable capabilities</td></tr>
<tr><td>Alternate mode support</td><td>The USB Power Delivery Structured VDMs are defined to extend the functionality a device exposes.</td></tr>
<tr><td>VCONN input Over-Voltage Protection</td><td>6V</td></tr>
<tr><td>Supporting VCONN with programmable OCP</td><td>Default: 400mA
VCONN level: 200mA~800mA, 100mA/step</td></tr>
<tr><td>Dead battery support</td><td>CC always is RD mode when dead battery</td></tr>
<tr><td>BMC BIST mode supported</td><td>BMC Built in Self-Test</td></tr>
<tr><td>Supported PD 3.0</td><td>Support Universal Serial Bus Power Delivery Specification 3.0</td></tr>
</table>

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General Function Index

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- Flash LED part
- Backlight LED part
- Display Bias part
- RGB part
- LDO part
- PD part

OTP

Over Temperature Protection

OTP function

- An Over-Temperature Protection (OTP) is featured in the device. The protection is triggered to force device shutdown when the junction temperature exceeds 160°C typically, the protection function is started and selection channels to turned off by (0x0F, bit[7:4]).
- The OTP specifications are shown below:

Parameter	Symbol	Test Conditions	Min	TYP	Max	Unit
Over-Temperature Protection Threshold	T_{OTP}	Thermal shutdown threshold temperature	-	160	-	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}	Thermal shutdown hysteresis temperature	-	20	-	°C

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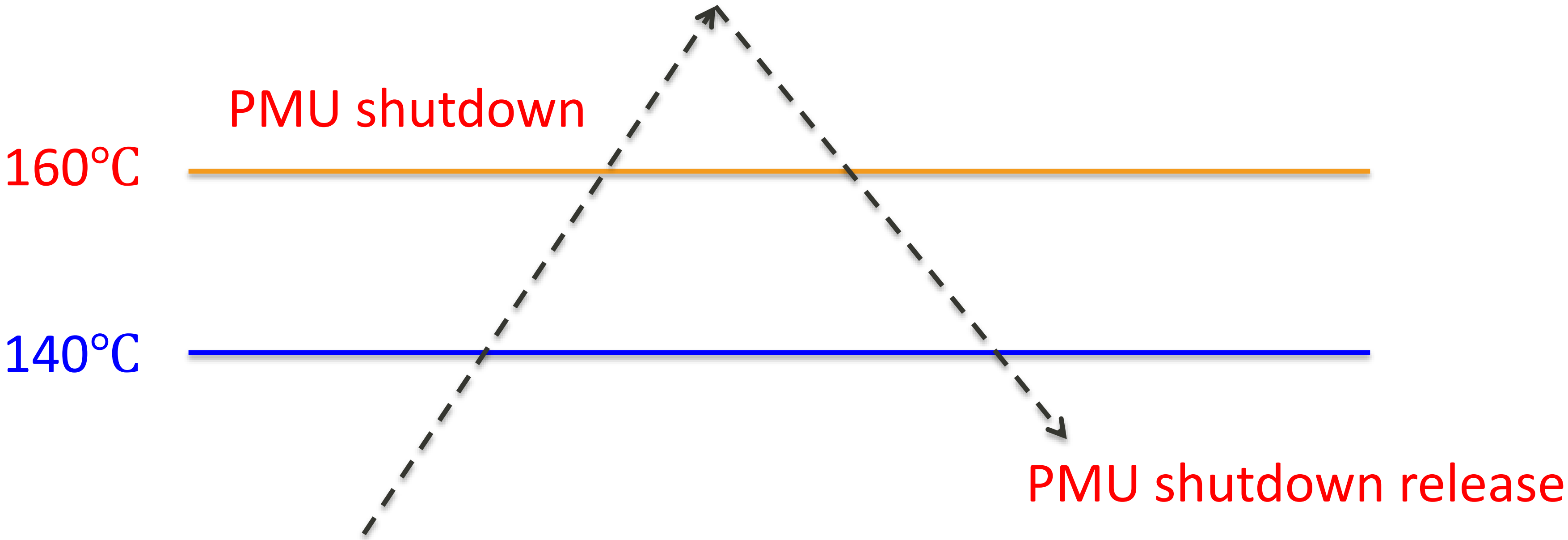
OTP function

- HW control (+/- 20 ℃)
  - HW shutdown release when Tj < 140 ℃
  - Tj>160 ℃ PMU HW shutdown
  - Thermal shutdown disable



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OTP function

- In some application case, the user maybe not want to turn-off all channels when OTP be triggered. We can select specific shutdown channel by set OT_SHDN_SEL via I^2C.

- Default is shutdown BL/DB/RGB/LDO and shutdown channel can be selected

Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x0F	SHDN_CTRL2	7:4	OT_SHDN_SEL	1111	RW	OT shutdown selection (will disable channels and set sEN_CHx=0) 0000 : Disable OTP shutdown function. 0001 : Enable shutdown function and shutdown LDO only 0010 : Enable shutdown function and shutdown RGB only 0011 : Enable shutdown function and shutdown RGB / LDO 0100 : Enable shutdown function and shutdown DB only 0101 : Enable shutdown function and shutdown DB/LDO 0110 : Enable shutdown function and shutdown DB/RGB 0111 : Enable shutdown function and shutdown DB/RGB/LDO 1000 : Enable shutdown function and shutdown BL only 1001 : Enable shutdown function and shutdown BL/LDO 1010 : Enable shutdown function and shutdown BL/RGB 1011 : Enable shutdown function and shutdown BL/RGB/LDO 1100 : Enable shutdown function and shutdown BL/DB 1101 : Enable shutdown function and shutdown BL/DB/LDO 1110 : Enable shutdown function and shutdown BL/DB/RGB 1111 : Enable shutdown function and shutdown BL/DB/RGB/LDO
		3:0	Reserved	0000	RW	Keep default value

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VDDA UVLO

VDDA UVLO

- The device provides an VDDA under-voltage protection (UVP, VDDA < 2.4V), the protection function is started and selection channels to turned off by (0x0E, bit[7:4]).
- The VDDA UVLO specifications are shown below:

Parameter	Symbol	Test Conditions	Min	TYP	Max	Unit
VDDA Under-Voltage Protection Threshold	V_{VDDA_UVLO}	VDDA falling	2.3	2.4	2.5	V
VDDA Under-Voltage Protection Hysteresis	$V_{VDDA_UVLO_HYS}$	VDDA rising	-	0.1	-	V

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VDDA UVLO

- In some application case, the user maybe not want to turn-off all channels when VDDA UVLO be triggered. We can select specific shutdown channel by set VDDAUV_SHDN_SEL via I^2C.

- Default is Disable VDDA UVLO shutdown function and shutdown channel can be selected

0x0E	SHDN_CTRL1	7:4	VDDAUV_SHDN_SEL	0000	RW	VDDA UVLO shutdown selection (will disable channels and set sEN_CHx = 0) 0000 : Disable VDDA UVLO shutdown function. 0001 : Enable shutdown function and shutdown LDO only 0010 : Enable shutdown function and shutdown RGB only 0011 : Enable shutdown function and shutdown RGB / LDO 0100 : Enable shutdown function and shutdown DB only 0101 : Enable shutdown function and shutdown DB / LDO 0110 : Enable shutdown function and shutdown DB / RGB 0111 : Enable shutdown function and shutdown DB / RGB / LDO 1000 : Enable shutdown function and shutdown BL only 1001 : Enable shutdown function and shutdown BL / LDO 1010 : Enable shutdown function and shutdown BL / RGB 1011 : Enable shutdown function and shutdown BL / RGB / LDO 1100 : Enable shutdown function and shutdown BL / DB 1101 : Enable shutdown function and shutdown BL / DB / LDO 1110 : Enable shutdown function and shutdown BL / DB / RGB 1111 : Enable shutdown function and shutdown BL / DB / RGB / LDO

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VDDA OVP

VDDA OVP

- The device provides an VDDA over-voltage protection (OVP, VDDA > 5.95V), the protection function is started and selection channels to turned off by (0x0E, bit[3:0]
- The VDDA OVP specifications are shown below:

Parameter	Symbol	Test Conditions	Min	TYP	Max	Unit
VDDA Over-Voltage Protection Threshold	V_{VDDA_OVP}	VDDA rising	5.7	5.95	6.2	V
VDDA Over-Voltage Protection Hysteresis	$V_{VDDA_OVP_HYS}$	VDDA falling	-	0.2	-	V

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VDDA OVP

- In some application case, the user maybe not want to turn-off all channels when VDDA OVP be triggered. We can select specific shutdown channel by set VDDAOVP_SHDN_SEL via I^2C.

- Default is Disable VDDA OVP shutdown function and shutdown channel can be selected

Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x0E	SHDN_CTRL1	3:0	VDDAOVP_SHDN_SEL	0000	RW	VDDA OVP shutdown selection (will disable channels and set sEN_CHx=0) 0000 : Disable VDDA OVP shutdown function. 0001 : Enable shutdown function and shutdown LDO only 0010 : Enable shutdown function and shutdown RGB only 0011 : Enable shutdown function and shutdown RGB / LDO 0100 : Enable shutdown function and shutdown DB only 0101 : Enable shutdown function and shutdown DB / LDO 0110 : Enable shutdown function and shutdown DB / RGB 0111 : Enable shutdown function and shutdown DB / RGB / LDO 1000 : Enable shutdown function and shutdown BL only 1001 : Enable shutdown function and shutdown BL / LDO 1010 : Enable shutdown function and shutdown BL / RGB 1011 : Enable shutdown function and shutdown BL / RGB / LDO 1100 : Enable shutdown function and shutdown BL / DB 1101 : Enable shutdown function and shutdown BL / DB / LDO 1110 : Enable shutdown function and shutdown BL / DB / RGB 1111 : Enable shutdown function and shutdown BL / DB / RGB / LDO

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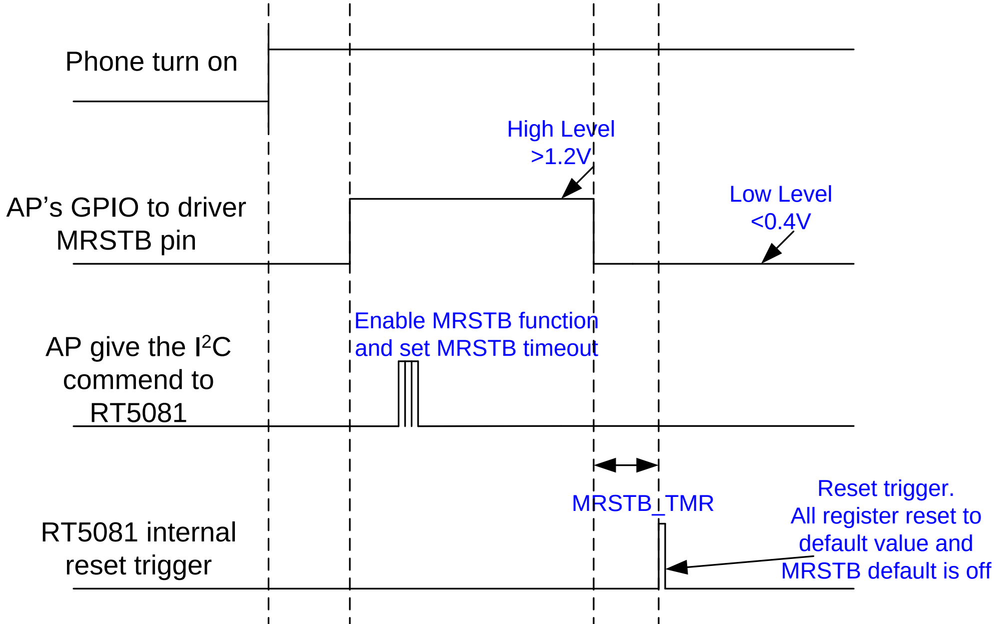
MRSTB

MRSTB pin

- The device provides a MRSTB pin for manual reset the hardware or register only.
- This function must be enabled by 0x01 [4]=1, select de-bouncing time by 0x01 [3:1] and select reset method by 0x01 [0].

0x01[4]	Description
MREN=0	Disable (Default)
MREN=1	Enable (MRSTB pull low will start MRSTB Timer counting)
0x01[0]	**Reset Method**
MRSTB_RST_SEL=0	Reset Hardware (Default)
MRSTB_RST_SEL=1	Reset Register only

0x01 3:1	MRSTB_TMR	011	RW	MRSTB debounce time selection 000: 0.75 ms 001: 1 ms 010: 1.25 ms 011: 1.5 ms Default 100: 1.75 ms 101: 2 ms 110: 2.25 ms 111: 2.5 ms



MRSTB Function

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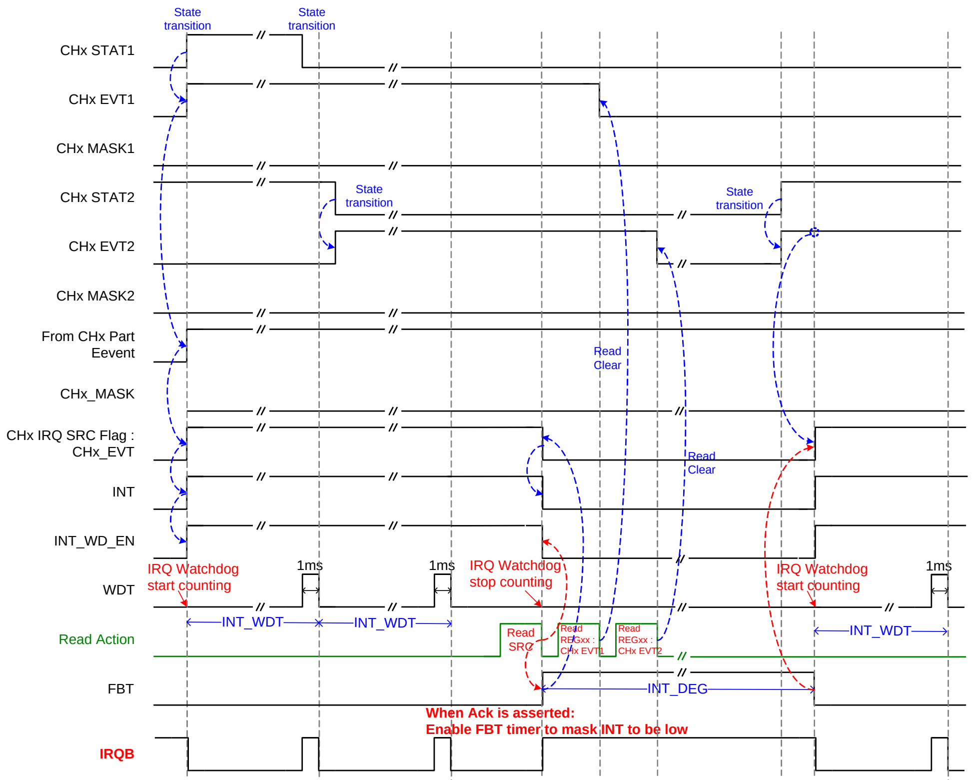
IRQ Watchdog

IRQ Watchdog

- To prevent interrupt event be missed, the RT5081 also provide IRQ Watchdog Timer function which can be enabled and set by 0x0D (bit 7 – 6).

Bit	Bit Name	Default	Type	Description
0x0D 7:6	INT_WDT	00	RW	Interrupt Watchdog timer. 00: Disabled (Default) 01 : 250ms 10 : 500ms 11 : 1000ms

IRQ Watchdog :



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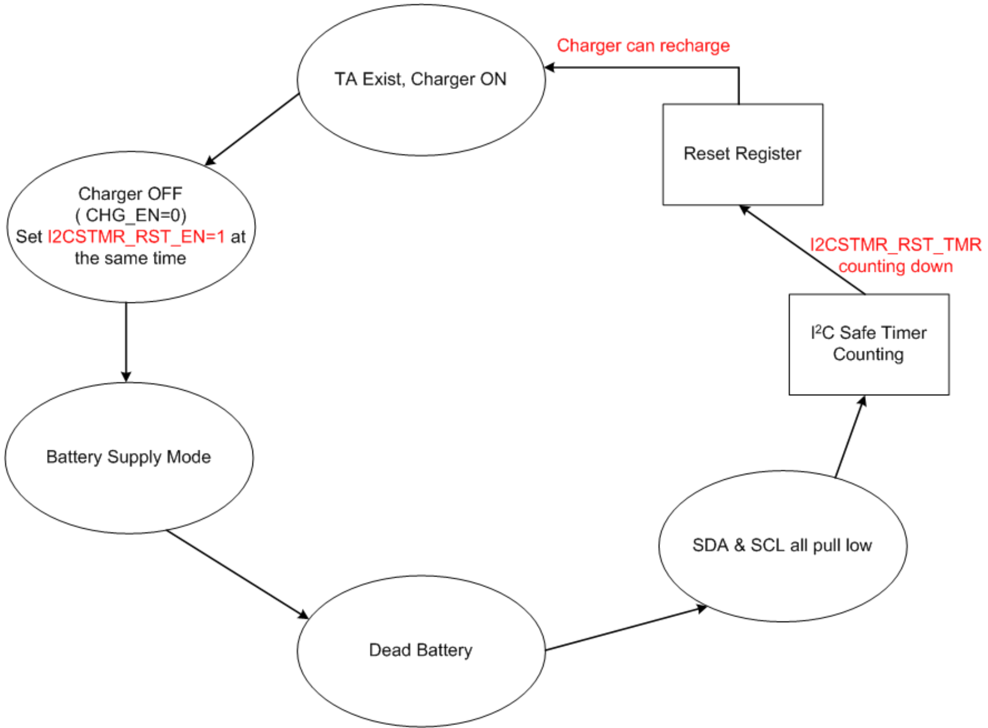
I^2C Safe Timer

I^2C Safe Timer

- When system freeze and charger be disabled. Battery will keep consumption and become to dead battery.
- To prevent this situation. The RT5081 also provide I^2C Safe Timer function which can be enabled by set 0x01 (Bit7) and set safe timer deglitch time by 0x01 (bit 6 - 5).

0x07[7]	Description
I2CSTMR_RST_EN=0	Disable safe timer(Default)
I2CSTMR_RST_EN=1	Enable safe timer

0x01 6:5	I2CSTMR_RST_TMR	00	RW	I^2C Safe Timer deglitch time. 00: 0.5 Sec Default 01: 0.75 Sec 10: 1 Sec 11: 2 Sec



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- Backlight LED part
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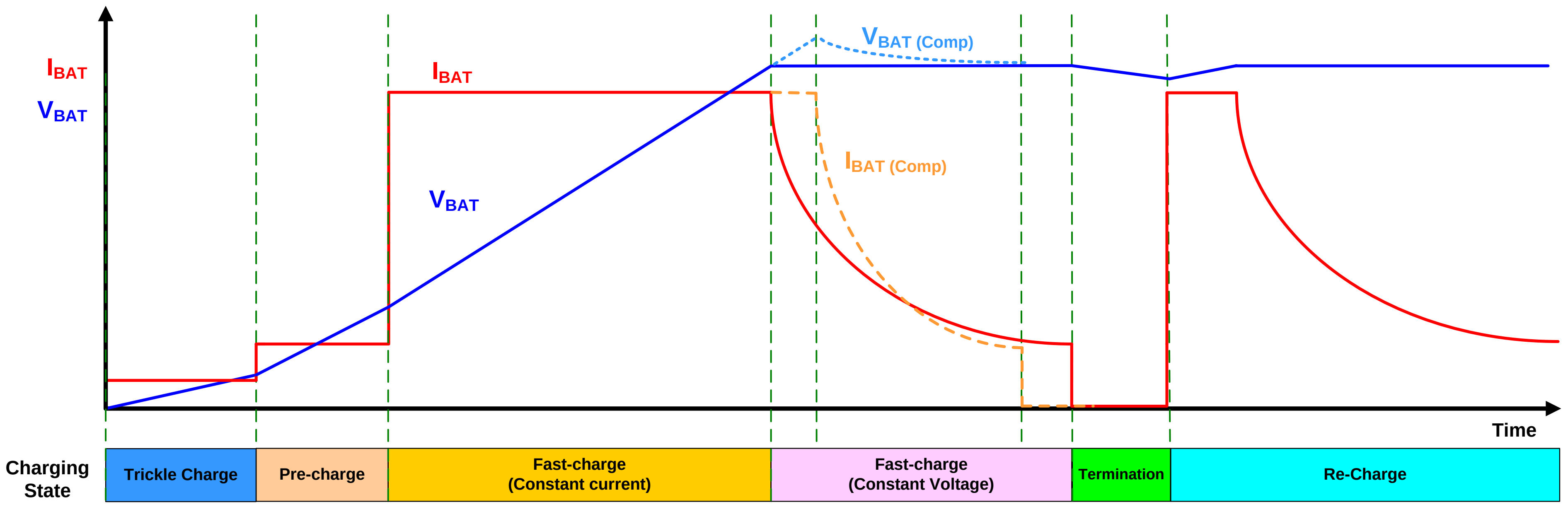
- RGB part
- LDO part
- PD part

Charger Enable and Charger Procedure

Charge Profile

- There are 5 intervals for total charging

1. It depends on battery voltage level to change charging state
2. It includes trickle charge when VBAT is over discharged
3. RT5081 features IR compensation(Resistance compensation from charger to battery connector) and Termination in constant voltage mode



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Charge State – Trickle Charge

- Trickle charge

1. VBAT < 2V, the charging current will change to 100mA automatically.
2. The trickle charge current and voltage level are can not be programmable.

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Charge State – Pre Charge

- Pre Charge

1. When VPREC (default=3V) > VBAT > 2V, the charging current will increase to pre-charge current (default = 150mA) level which set by register.
2. For system boot up consideration, VSYS will be regulated by system minimum level (default = 3.6V) which can be programmed by I^2C

Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x18	CHG_CTRL8	7:4	VPREC	1010	RW	Pre-charge voltage threshold (Rising) 0000 : 2V 0001 : 2.1V 0010 : 2.2V 0011 : 2.3V 0100 : 2.4V 0101 : 2.5V 0110 : 2.6V 0111 : 2.7V 1000 : 2.8V 1001 : 2.9V 1010 : 3.0V 1011 : 3.1V 1100 : 3.2V 1101 : 3.3V 1110 : 3.4V 1111 : 3.5V
		3:0	IPREC	0001	RW	Pre-charge current level 0000 : 100mA 0001 : 150mA 0010 : 200mA 0011 : 250mA 0100 : 300mA 0101 : 350mA 0110 : 400mA 0111 : 450mA 1000 : 500mA 1001 : 550mA 1010 : 600mA 1011 : 650mA 1100 : 700mA 1101 : 750mA 1110 : 800mA 1111 : 850mA

Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x1B	CHG_CTRL11	7	ADP_DIS	0	RW	Charger adapter detection disable 0 : Adapter detection is enable 1 : Adapter detection is disabled
		6	BATD_EN	0	RW	Charger battery detection when charge done 0 : Battery detection is disabled 1 : Battery detection is enabled
		5	SYSUV_HW_SEL	1	RW	System UV protection selection bit 0 : Switching is not turned off when System UVP 1 : Switching is turned off when System UVP
		4:2	SYSREG	011	RW	System minimum regulation voltage 000 : 3.3V 001 : 3.4V 010 : 3.5V 011 : 3.6V 100 : 3.7V 101 : 3.8V 110 : 3.9V 111 : 4.0V
		1:0	VRECH	00	RW	Charging re-charge voltage threshold with VOREG 00 : 100mV 01 : 200mV 10 : 300mV 11 : 400mV

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Charge State – Constant Current

- Fast Charge

1. After VBAT > VPREC (default = 3V), the charging current will decided by main charging factor. (Explain by page 46 to 54)
2. The charging current is programmable from 0.1 to 5A. (default = 2A)

Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x18	CHG_CTRL8	7:4	VPREC	1010	RW	Pre-charge voltage threshold (Rising) 0000 : 2V 0001 : 2.1V 0010 : 2.2V 0011 : 2.3V 0100 : 2.4V 0101 : 2.5V 0110 : 2.6V 0111 : 2.7V 1000 : 2.8V 1001 : 2.9V 1010 : 3.0V 1011 : 3.1V 1100 : 3.2V 1101 : 3.3V 1110 : 3.4V 1111 : 3.5V
		3:0	IPREC	0001	RW	Pre-charge current level 0000 : 100mA 0001 : 150mA 0010 : 200mA 0011 : 250mA 0100 : 300mA 0101 : 350mA 0110 : 400mA 0111 : 450mA 1000 : 500mA 1001 : 550mA 1010 : 600mA 1011 : 650mA 1100 : 700mA 1101 : 750mA 1110 : 800mA 1111 : 850mA

Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x17	CHG_CTRL7	7:2	ICHG	010011	RW	Regulated charge current 000000 : 0.1A 000001 : 0.2A 000010 : 0.3A ... 001000 : 0.9A 001001 : 1A 001010 : 1.1A ... 010010 : 1.9A 010011 : 2A ... 011100 : 2.9A 011101 : 3A ... 100110 : 3.9A 100111 : 4A ... 110000 : 4.9A 110001 : 5A 110010~111111 : 5A
		1:0	EOC_TIMER	00	RW	EOC back-charging time 00 : 0mins 01 : 30mins 10 : 45mins 11 : 60mins

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Charge State – Constant Voltage

- Fast Charge

3. After VBAT >= VOREG (default = 4.2V), the charging current will decreased
4. The user can select enable IR compensation or not. (default = 0m ohm, explain by page 42 to 44)

Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x14	CHG_CTRL4	7:1	VOREG	0011110	RW	Battery regulation voltage. The delta-V of the battery regulation voltage is 10mV. 0000000 : 3.9V 0000001 : 3.91V 0000010 : 3.92V 0000011 : 3.93V … 0011101 : 4.19V 0011110 : 4.2V 0011111 : 4.21V … 0101100 : 4.34V 0101101 : 4.35V 0101110 : 4.36V … 1010001 : 4.71V 1010001~1111111 : 4.71V
		0	Reserved	0	RW	Keep default value

Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x2C	CHG CTRL 18	7:6	Reserved	01	RW	Reserved
		5:3	BAT_COMP	000	RW	Battery IR compensation resistor setting 000 : 0mΩ 001 : 25mΩ 010 : 50mΩ 011 : 75mΩ 100 : 100mΩ 101 : 125mΩ 110 : 150mΩ 111 : 175mΩ
		2:0	VCLAMP	000		Battery IR compensation maximum voltage clamp 000 : 0mV 001 : 32mV 010 : 64mV 011 : 96mV 100 : 128mV 101 : 160mV 110 : 192mV 111 : 224mV

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Charge State – Termination

- Termination

1. When charging current < IEOC level (default = 250mA), after during deglitch time (default = 2ms), the RT5081 will send IEOC IRQ.

Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x19	CHG_CTRL9	7:4	IEOC	0011	RW	End-of-charge current (IEOC) setting 0000 : 100mA 0001 : 150mA 0010 : 200mA 0011 : 250mA 0100 : 300mA 0101 : 350mA 0110 : 400mA 0111 : 450mA 1000 : 500mA 1001 : 550mA 1010 : 600mA 1011 : 650mA 1100 : 700mA 1101 : 750mA 1110 : 800mA 1111 : 850mA
		3	EOC_EN	1	RW	IEOC (charge current termination) enable/disable 0: Disable 1: Enable
		2:0	CHG_TDEG_EOC	100	RW	EOC deglitch time 000 : 32us 001 : 64us 010 : 128us 011 : 256us 100 : 2ms 101 : 4ms 110 : 8ms 111 : 16ms

Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x19	CHG_CTRL9	7:4	IEOC	0011	RW	End-of-charge current (IEOC) setting 0000 : 100mA 0001 : 150mA 0010 : 200mA 0011 : 250mA 0100 : 300mA 0101 : 350mA 0110 : 400mA 0111 : 450mA 1000 : 500mA 1001 : 550mA 1010 : 600mA 1011 : 650mA 1100 : 700mA 1101 : 750mA 1110 : 800mA 1111 : 850mA
		3	EOC_EN	1	RW	IEOC (charge current termination) enable/disable 0: Disable 1: Enable
		2:0	CHG_TDEG_EOC	100	RW	EOC deglitch time 000 : 32us 001 : 64us 010 : 128us 011 : 256us 100 : 2ms 101 : 4ms 110 : 8ms 111 : 16ms

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Charge State – Termination

- Termination

1. After IEOC IRQ occurs, the charger behavior decided by I^2C bit TE (default = disabled)
2. If TE = 1, charger will stop charging battery
3. If TE = 0, charger will keep charging battery

Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x12	CHG_CTRL2	7	SHIP_MODE	0	RW	Shipping mode enable, force BATFET OFF 0 : Allow BATFET turn on 1 : Force BATFET turn off
		6	BATDET_DIS_DLY	0	RW	BATFET turn off delay 0 : BATFET turn off immediately 1 : BATFET turn off with 10s delay after SHIP_MODE bit is set
		5	BYPASS_MODE	0	RW	Bypass mode enable, disable Buck but force BATFET on 0 : Bypass mode disable 1 : Bypass mode enable
		4	TE	0	RW	Termination enable 0 : Disable charge current termination 1 : Enable charge current termination
		3:2	IINLMTSEL	00	RW	Input current limit selection bit 00 : AICR=3.25A 01 : CHG_TYP results is applied 10 : IAICR[5:0] results is applied 11 : Input limit is set by the lower level of these three
		1	CFO_EN	1	RW	Charger and OTG enable 0 : CFO is disabled 1 : CFO is enabled
		0	CHG_EN	1	RW	Charging enable 0 : CHG is disabled 1 : CHG is enabled

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Charge State – Re Charge

- Re Charge

1. Once if VBAT is lower than VOREG – VREC (default = 100mV), the RT5081 will start to charging battery
2. Charging behavior is back to constant current state

Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x1B	CHG_CTRL11	7	ADP_DIS	0	RW	Charger adapter detection disable 0 : Adapter detection is enable 1 : Adapter detection is disabled
		6	BATD_EN	0	RW	Charger battery detection when charge done 0 : Battery detection is disabled 1 : Battery detection is enabled
		5	SYSUV_HW_SEL	1	RW	System UV protection selection bit 0 : Switching is not turned off when System UVP 1 : Switching is turned off when System UVP
		4:2	SYSREG	011	RW	System minimum regulation voltage 000 : 3.3V 001 : 3.4V 010 : 3.5V 011 : 3.6V 100 : 3.7V 101 : 3.8V 110 : 3.9V 111 : 4.0V
		1:0	VRECH	00	RW	Charging re-charge voltage threshold with VOREG 00 : 100mV 01 : 200mV 10 : 300mV 11 : 400mV

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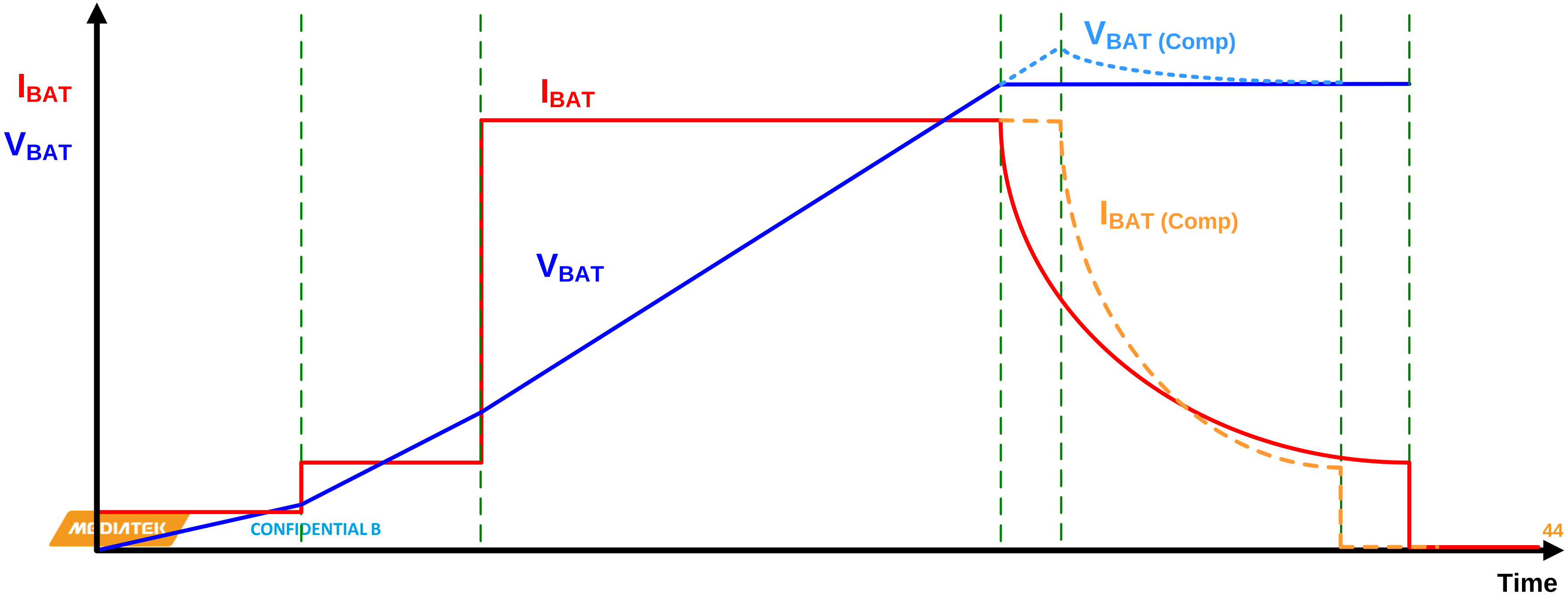
Analog IR Drop Compensation

Analog IR Drop Compensation

- IR Compensation

1. Compensate the resistance of RT5081 to battery connector path
2. The IR compensation can speed up the total charging time
3. In order to protect battery, RT5081 features Battery OVP function. OVP level is decided by VOREG*108%
4. After trigger BATOVP, charger will stop charging battery but power path keeps turn on for system loading. Same as TI's method.



CONFIDENTIAL B

Analog IR Drop Compensation

- IR Compensation

1. The compensate voltage is decided by minimum of (VCLAMP & Charging Current x BAT_COMP)
2. VCLAMP (default = 0mV), BAT_COMP (default = 0m ohm)
3. CHG_VBATOVPB Pin (Open-drain)

   Low : Event occurs, High : No operation

Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x2C	CHG CTRL 18	7:6	Reserved	01	RW	Reserved
		5:3	BAT_COMP	000	RW	Battery IR compensation resistor setting 000 : 0mΩ 001 : 25mΩ 010 : 50mΩ 011 : 75mΩ 100 : 100mΩ 101 : 125mΩ 110 : 150mΩ 111 : 175mΩ
		2:0	VCLAMP	000		Battery IR compensation maximum voltage clamp 000 : 0mV 001 : 32mV 010 : 64mV 011 : 96mV 100 : 128mV 101 : 160mV 110 : 192mV 111 : 224mV

Enable Bits for Charger

- There are 3 enable bits, related to the charger.

  1.CFO_EN (default = Enable) :

  - This bit is used to enable or disable the buck and boost of charger.
  - Note: When disable CFO_EN, the power path still be turned-on. Buck be turned-off

  2.CHG_EN (default = Enable) :

  - When CHG_EN = Disabled
    - Zero charging current
    - System loading provided by input source.
    - Note: power path be turned-off
    - Once if ISYS > IIN, battery will provide system loading to prevent VSYS voltage drop.
  - The CHG_EN bit function is the same as CHG_ENB pin.

  3.HZ (default = Disabled) :

  - Turn off most of the charger internal circuits.
  - Cable plug-in will exit HZ mode.

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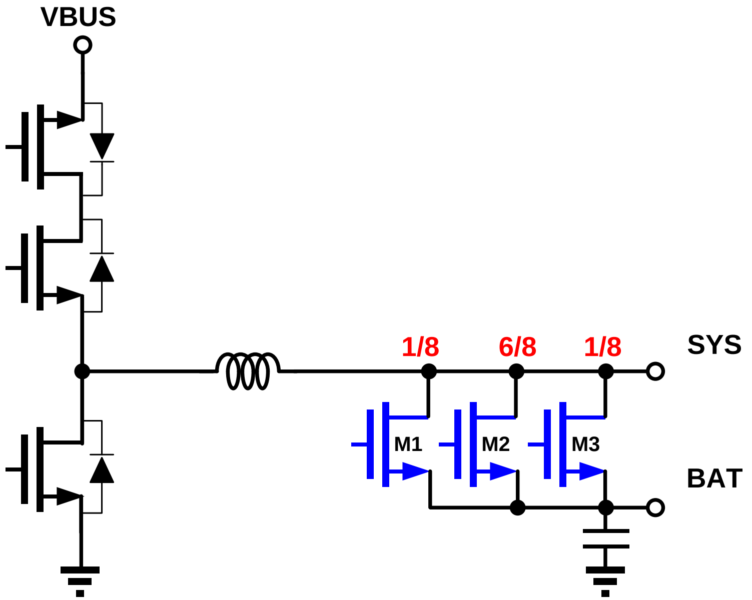
Power Path Circuit Design

Power Path Circuit Design

1. In order to guarantee stability (ICC = 0.1 to 5A)
2. Normal Charging (ICC>=900mA), the power path is fully on. But in low charging current (ICC < 900mA), the power path will partially turn on.

- When ICC >= 900mA, the power path is fully turn on. Ron is 13mOhm(typ), OCP=15A.
- When 800mA > ICC >= 500mA, the power path is partially turn on, (2/8). Ron is 50mOhm(typ), OCP is 6A.
- When 400mA >= ICC, the power path is partially turn on, (1/8). Ron is 100mOhm(typ), OCP is 4.5A.



MIVR
(Minimum Input Voltage Regulation)

MIVR(Minimum Input Voltage Regulation)

- MIVR function as same as TI's VINDPM function to avoid VBUS voltage collapse to UVLO.
- Default is 4.4V and can be set as 3.9V~13.4V per 0.1V.

Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x16	CHG_CTRL6	7:1	VMIVR	0000101	RW	Input MIVR threshold setting 0000000 : 3.9V 0000001 : 4V 0000010 : 4.1V 0000011 : 4.2V 0000100 : 4.3V 0000101 : 4.4V 0000110 : 4.5V … 0011110 : 6.9V 0011111: 7V … 0110010 : 8.9V 0110011 : 9V … 1010000 : 11.9V 1010001 : 12V … 1011111 : 13.4V 1100000~1111111: 13.4V
		0	MIVR_EN	1	RW	MIVR loop enable 0 : MIVR loop disable 1 : MIVR loop enable

AICR
(Average Input Current Regulation)

AICR(Average Input Current Regulation)

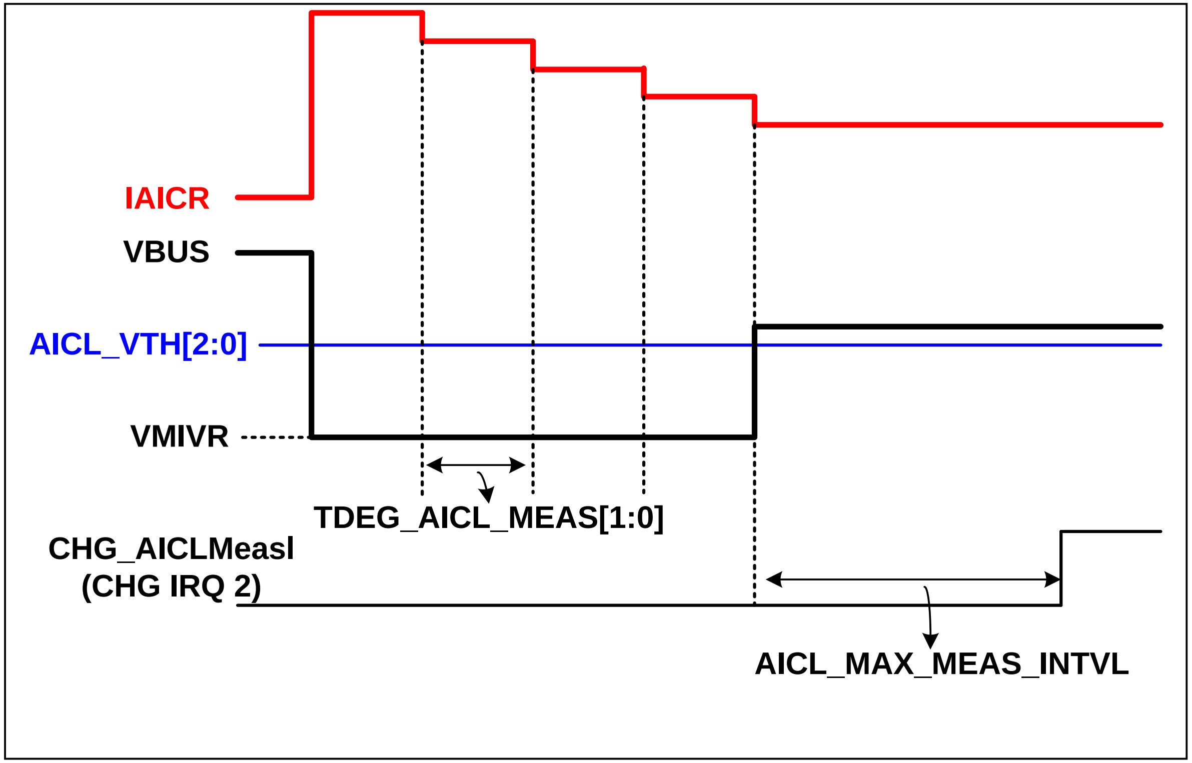
- AICR function as same as TI's IINLIM function
- Default is 500mA and can be set as 100mA~3.25A per 50mA.
- Auto set the AICR level of current pattern when enable PE+1.1 and PE+2.0 communication

Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x13	CHG_CTRL3	7:2	IAICR	001000	RW	AICR setting 000000 : 100mA 000001 : 150mA 000010 : 200mA 000011 : 250mA ... 001000 : 500mA 001001 : 550mA ... 100110 : 2A ... 111010 : 3A ... 111111 : 3.25A
		1	AICR_EN	1	RW	AICR loop enable 0 : AICR loop disable 1 : AICR loop enable
		0	ILIM_EN	1	RW	ILIM function enable 0 : ILIM function disable 1 : ILIM function enable

AICL
(Average Input Current Level)

AICL(Average Input Current Level)

- AICL function as like as TI's ICO function
- AICL_VTH – VMIVR should be larger than 0.2V
- When IAICR set to large current and the VBUS drop to VMIVR level, AICL measurement will decrease IAICR level step by step automatically until VBUS voltage is large than AICL threshold voltage.



Input Current Limit Setting

Input Current Limit Setting

- In fast-charge mode, the input current limit can be selected by IINLMTSEL .
- The actual input current limit is decided by the lowest one of IINLMTSEL and CHG_ILIM pin current limit.

Addr	RegName	Bit	BitName	Default	Description
0x12	CHG_CTRL2	3:2	IINLMTSEL[1:0]	00	Input current limit selection bit 00 : AICR=3.25A (default) 01 : CHG_TYP results is applied 10 : IAICR[5:0] results is applied 11 : Input limit is set by the lower level of these three

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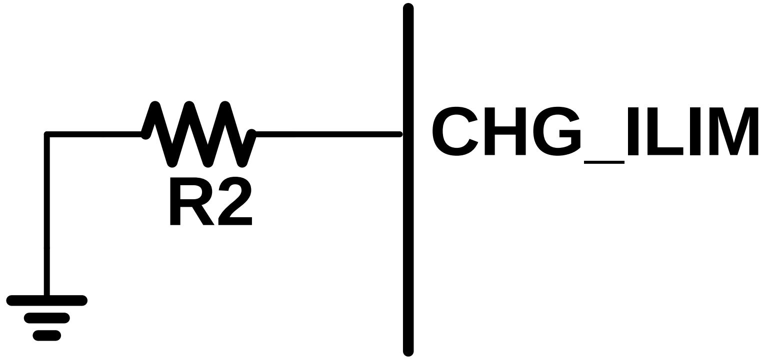
GHG_ILIM PIN Setting

- For hardware protection, the PMIC supports input current limit on CHG_ILIM pin which set by a resistor (R2) from CHG_ILIM pin to ground.
- Formula : IINMAX = KILIM / RILIM

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Unit
Input Current Limit Factor	K_{ILIM_CHG}	Input current regulation by CHG_ILIM pin = 1.5A	320	355	390	AΩ



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Charger Watchdog

Charger Watchdog

- The host has to reset the watchdog timer by writing or reading by I^2C periodically
- When the watchdog timer is expired, IC will set Register as below:
  - (1)CFO_EN disable
  - (2)CHG_EN disable
  - (3)Return to charge mode (Exit OTG mode, and reset entry method of OTG)
  - (4)Enable safety timer

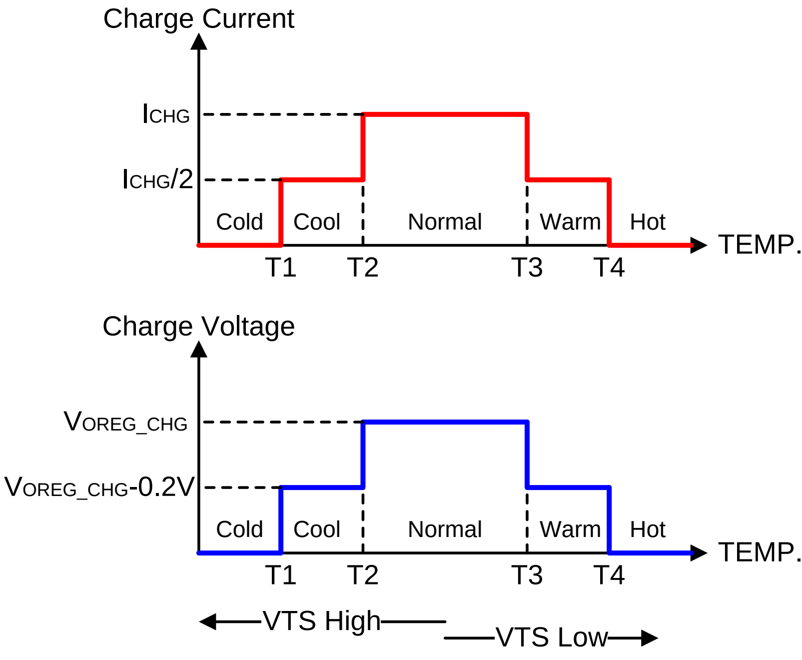
Address	Bit	Bit Name	Description
0x1D	7	CHG_WDT_EN	Charger Watch dog timer enable/disable 0 : Disable(default) 1 : Enable
	6	CHG_WDT_TRST	Waiting timer to set Register after watchdog is asserted 0 : 200ms 1 : 500ms(default)
	5:4	CHG_WDT	Watch dog timer, from WDTEN is enabled to watchdog IRQ 00 : 8s 01 : 40s(default) 10 : 80s 11 : 160s

JEITA Setting

JEITA Setting

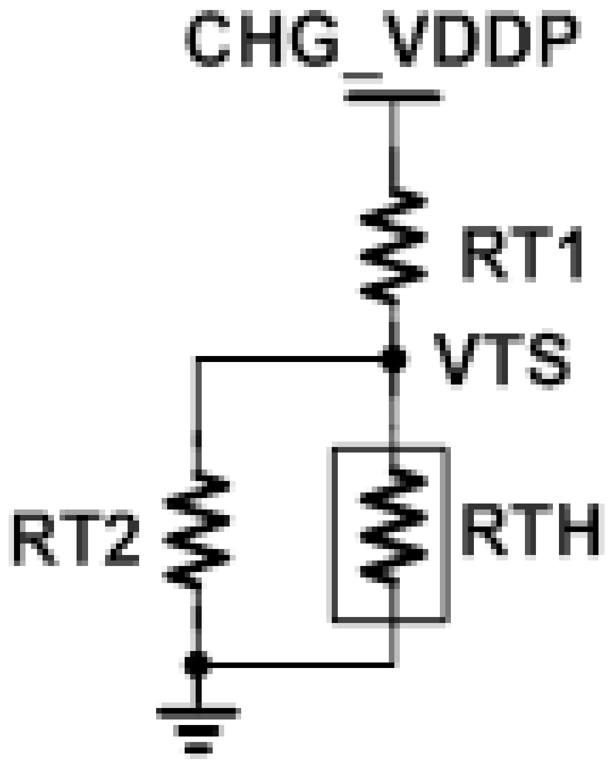
- There are 5 regions for JEITA protection, as below table.
- When temperature in warm or cool region, charging current and voltage can be selected.

Region	Threshold (Typical Value)	Charging current	Charging voltage
HOT Threshold	the ratio of VLDO < 34.5%	Stop charging	Stop charging
WARM Threshold	the ratio of VLDO < 45%	ICHG,ICHG/2 (default=ICHG/2) Reg0x20 (bit2)	VOREG,VOREG-0.2V (default=VOREG-0.2V)) Reg0x20 (bit0)
NORMAL Threshold	45%<the ratio of VLDO < 68.5%	ICHG	VOREG
COOL Threshold	the ratio of VLDO > 68.5%	ICHG,ICHG/2 (default=ICHG/2) Reg0x20 (bit3)	VOREG,VOREG-0.2V (default=VOREG-0.2V) Reg0x20 (bit1)
COLD Threshold	the ratio of VLDO > 73.5%	Stop charging	Stop charging



JEITA Setting

- If customer want to disable this function by HW, please select RT1= 50kohm ,RT2=50kohm,RTH=Open.

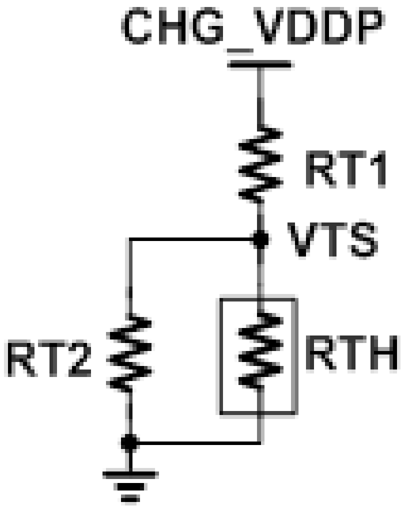


TS Pin Calculation

- Step1: Assuming a NTC thermistor on the battery pack as shown
- Step2 : Select 0°C to 60°C range for Li-ion battery, then find NTC thermistor resistance R_{Cold} and R_{Hot}
- Step3: the value RT1 and RT2 can be determined by using equations as below

$$R_{T1} = CHG_VDDP * [(1/ V_{T1} - 1/ V_{T4})/(1 / R_{Cold} – 1 / R_{Hot})] – (1)$$

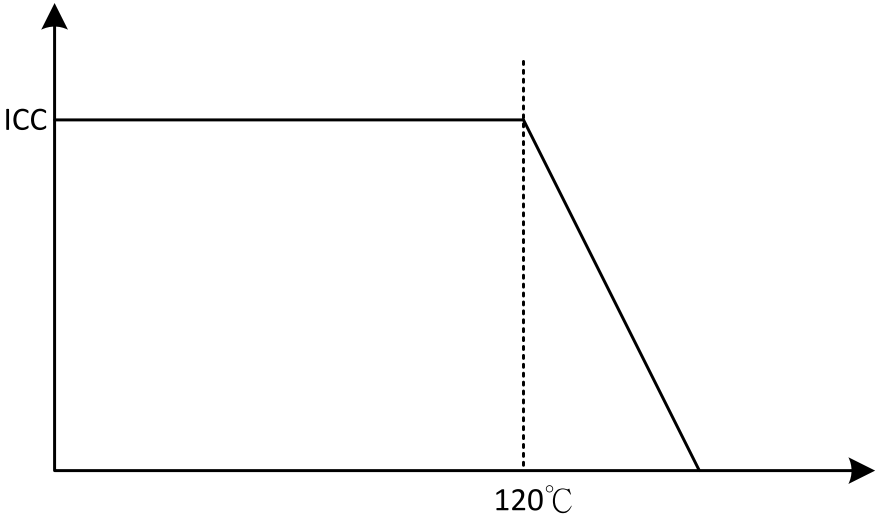
$$R_{T2} = R_{T1} * [1 / (CHG_VDDP / V_{T1} - R_{T1} / R_{Cold} - 1)] – (2)$$



Thermal Regulation Setting

Thermal Regulation Setting

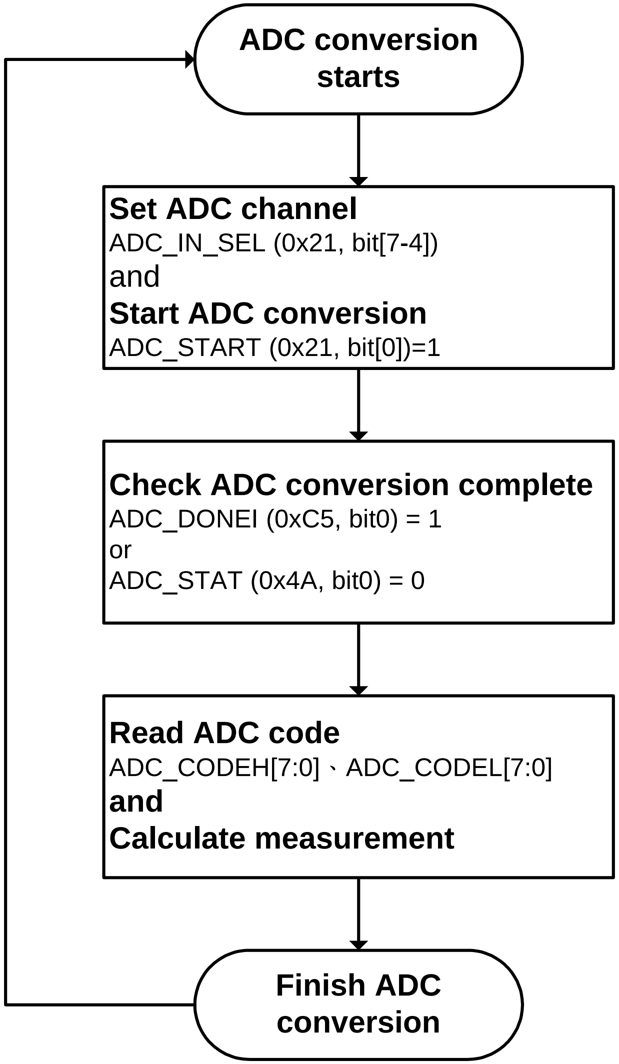
- RT5081 has four levels for thermal regulation setting
  - THREG: 60°C, 80°C, 100°C, 120°C.
- When RT5081 reach thermal regulation setting, it will start to decrease charging current and send TREG IRQ.



Address	Reg Name	Bit	Bit Name	Default	Type	Description
0xC0	CHG_IRQ1	7	PWR_RDY_EVT	0	R	Power ready detection result : Input power is good, UVLO < VIN < VOVP & VIN > BATS + VSLP 0 : No operation 1 : Event occurs
		6	CHG_MIVR_EVT	0	R	Charger warning. Input voltage MIVR loop active. 0 : No operation 1 : Event occurs
		5	CHG_AICR_EVT	0	R	Charger warning. Input current AICR loop active. 0 : No operation 1 : Event occurs
		4	CHG_TREG_EVT	0	R	Charger warning. Thermal regulation loop active. 0 : No operation 1 : Event occurs
		3:1	Reserved	000	R	Reserved
		0	DIRCHG_ON_EVT	0	R	LVHI is active or not (Rising/Falling trigger) 0 : LVHI is not active 1 : LVHI is active

ADC Setting

ADC Conversion Operation Flow



- The figure shows the flow chart of ADC conversion operation.
  - Select an ADC channel by setting **ADC_IN_SEL**
  - Enable **ADC_START**
  - Check ADC conversion complete by **ADC_DONI**
  - If **ADC_DONI** = “1”, Read ADC code **ADC_CODEH** and **ADC_CODEL**
  - Calculate and return result

ADC Measurement Equation and Range

- The table below shows measurement equations for various ADC channels.

ADC Channel	Measurement Equation	Measurement Range
VBUS_DIV5	[(ADC_CODEH x 256) + ADC_CODEL] * 25 mV	1V to 22V
VBUS_DIV2	[(ADC_CODEH x 256) + ADC_CODEL] * 10 mV	1V to 9.7V
VBAT	[(ADC_CODEH x 256) + ADC_CODEL] * 5 mV	0V to 4.9V
VSYS	[(ADC_CODEH x 256) + ADC_CODEL] * 5 mV	0V to 4.9V
CHG_VDDP	[(ADC_CODEH x 256) + ADC_CODEL] * 5 mV	0V to 4.9V
TS_BAT	[(ADC_CODEH x 256) + ADC_CODEL] * 0.25 %	0% to 100%
IBUS IAICR[5:0] setting < 400mA	[(ADC_CODEH x 256) + ADC_CODEL] * 50mA * 0.67	0A to 0.4A
IBUS IAICR[5:0] setting ≥ 400mA	[(ADC_CODEH x 256) + ADC_CODEL] * 50mA	0A to 5A
IBAT ICHG[5:0] setting 100mA to 450mA	[(ADC_CODEH x 256) + ADC_CODEL] * 50mA * 0.475	0A to 0.45A
IBAT ICHG[5:0] setting 500mA to 850mA	[(ADC_CODEH x 256) + ADC_CODEL] * 50mA * 0.536	0A to 0.85A
IBAT ICHG[5:0] setting ≥ 900mA	[(ADC_CODEH x 256) + ADC_CODEL] * 50mA	0A to 5A
TEMP_JC	[(ADC_CODEH x 256) + ADC_CODEL] * 2 °C -40°C	-40 to 120°C

Shipping Mode

Shipping Mode Setting

- Enable shipping mode by setting **SHIP_MODE**
  - RT5081 will shut down internal circuits to reduce quiescent current
  - BATFET to be turned off with a delay time **BATDET_DIS_DLY**

	Delay Time
BATDET_DIS_DLY=0	0s
BATDET_DIS_DLY=1	10s

- There are several ways to exit shipping mode

  HW
  - Input power source is plugged in
  - **CHG_QONB** pin is pulled from Logic High to Logic Low within 1 second

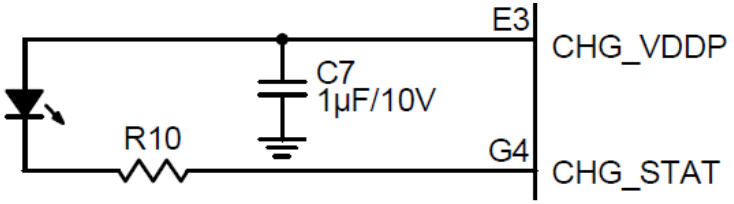
  SW
  - Disable **SHIP_MODE** bit
  - Enable **RST_REG** to reset all registers to default values

Charger Status

Charger Status

- There are two ways to check the RT5081's status:
  - CHG_STAT pin is an open-drain output to indicate charge status, which are summarized in Table for charge mode only.

Charger Status	CHG_STAT Pin Output
Charge is in progress	LOW
Charge is done	HIGH
Charge is disabled	HIGH
Any fault occurs	Blink at 1Hz



  - Status is indicated in the register **CHG_STAT** as below.

CHG_STAT 0x4A[7:6]	Charger Status
CHG_STAT=00	Ready
CHG_STAT=01	Charge is in progress
CHG_STAT=10	Charge is done
CHG_STAT=11	Fault

OTG Mode

OTG Mode

- There are two ways to enable OTG mode
  - Through I²C to set **OTG_PIN_EN**=0 and **OPA_MODE**=1
  - Through I²C to set **OTG_PIN_EN**=1, **OPA_MODE**=1 and **only** control **CHG_OTG** pin level to enter / exit OTG mode

OTG_PIN_EN (Bit = 1)	CHG_OTG (Pin = High)	CHG_OTG (Pin = Low)
OPA_MODE (Bit = 1)	Boost mode	Charger mode
OPA_MODE (Bit = 0)	Charger mode	Charger mode

OTG_PIN_EN (Bit = 0)	CHG_OTG (Pin = High)	CHG_OTG (Pin = Low)
OPA_MODE (Bit = 1)	Boost mode	Boost mode
OPA_MODE (Bit = 0)	Charger mode	Charger mode

OTG Mode

- RT5081 also provides **UUG_ON** bit, which can be applied to different applications
  - If **OTG mode** and **UUG_ON** are enabled

    The boost-mode output is on the VBUS pin, which can be used for OTG (On the Go) mode in mobile phones.
  - If **OTG mode** is enabled but **UUG_ON** bit is disabled

    The boost-mode output is on the CHG_VMID pin, which can be used in power banks. Adapter power can be delivered to PD (Powered Device) directly.

CHG_DSEL Pin

CHG_DSEL Pin

- The CHG_DSEL pin
  - Open-drain output type
  - This pin is used to indicated D+/D- detection status and type
  - When the device starts to detect input source
    - CHG_DSEL drives low → Detection is in progress.
  - When detection is completed,
    - This pin keeps low → DCP / HVDCP is detected.
    - This pin keeps high → SDP / CDP is detected.

Charger OCP(Over Current Protection)

Charger Over Current Protection

- Charger inductor peak current limit level
  - Charger OCP is a protection to prevent too high charging current or system loading
  - Once trigger charger OCP, the system regulation voltage will decrease for lock inductor current peak level immediately. Not hiccup type protection.
  - The current limit level (6A, 8A) can be programmed by register.

Buck OCP Current	$I_{BUCK_OCP_CHG}$	Addr 0x1D[2] Higher_OCP = 0 : 6A	--	6	--	A
		Addr 0x1D[2] Higher_OCP = 1 : 8A	--	8	-	A

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OTG LBP(Low Battery Protection) & OTG_OC(Over Current Protection)

OTG_Low Battery Protection

- OTG LBP setting
  - OTG LBP is a protection to prevent too low battery voltage.
  - Its protection type is trigger setting level then exit boost immediately.
  - The range is 2.3V to 3.8V. Per step is 100mV.
  - This function can be disabled or enabled by register setting.

Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x1A	CHG_CTRL10	7:4	LBP	0101	RW	Low battery protection voltage selection (falling edge threshold, hysteresis voltage=0.4V) 0000 : 2.3V 0001 : 2.4V 0010 : 2.5V 0011 : 2.6V 0100 : 2.7V 0101 : 2.8V 0110 : 2.9V 0111 : 3.0V 1000 : 3.1V 1001 : 3.2V 1010 : 3.3V 1011 : 3.4V 1100 : 3.5V 1101 : 3.6V 1110 : 3.7V 1111 : 3.8V
		3	LBP_EN	1	RW	Low battery protection enable/disable 0 : Disable 1 : Enable
		2:0	OTG_OC	000	RW	OTG overload threshold of UUG Current (Minimum) 000 : 0.5A 001 : 0.7A 010 : 1.1A 011 : 1.3A 100 : 1.8A 101 : 2.1A 110 : 2.4A 111 : 3A

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OTG_Over Current Protection

- OTG_OC setting
  - OTG_OC is protection to prevent short or heavy loading at VBUS pin.
  - Its protection type is hiccup, it will keep turn on 4ms and turn off 100ms.
  - The OTG_OC range is from 0.5A to 3A. It can be programmed by register.

Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x1A	CHG_CTRL10	7:4	LBP	0101	RW	Low battery protection voltage selection (falling edge threshold, hysteresis voltage=0.4V) 0000 : 2.3V 0001 : 2.4V 0010 : 2.5V 0011 : 2.6V 0100 : 2.7V 0101 : 2.8V 0110 : 2.9V 0111 : 3.0V 1000 : 3.1V 1001 : 3.2V 1010 : 3.3V 1011 : 3.4V 1100 : 3.5V 1101 : 3.6V 1110 : 3.7V 1111 : 3.8V
		3	LBP_EN	1	RW	Low battery protection enable/disable 0 : Disable 1 : Enable
		2:0	OTG_OC	000	RW	OTG overload threshold of UUG Current (Minimum) 000 : 0.5A 001 : 0.7A 010 : 1.1A 011 : 1.3A 100 : 1.8A 101 : 2.1A 110 : 2.4A 111 : 3A

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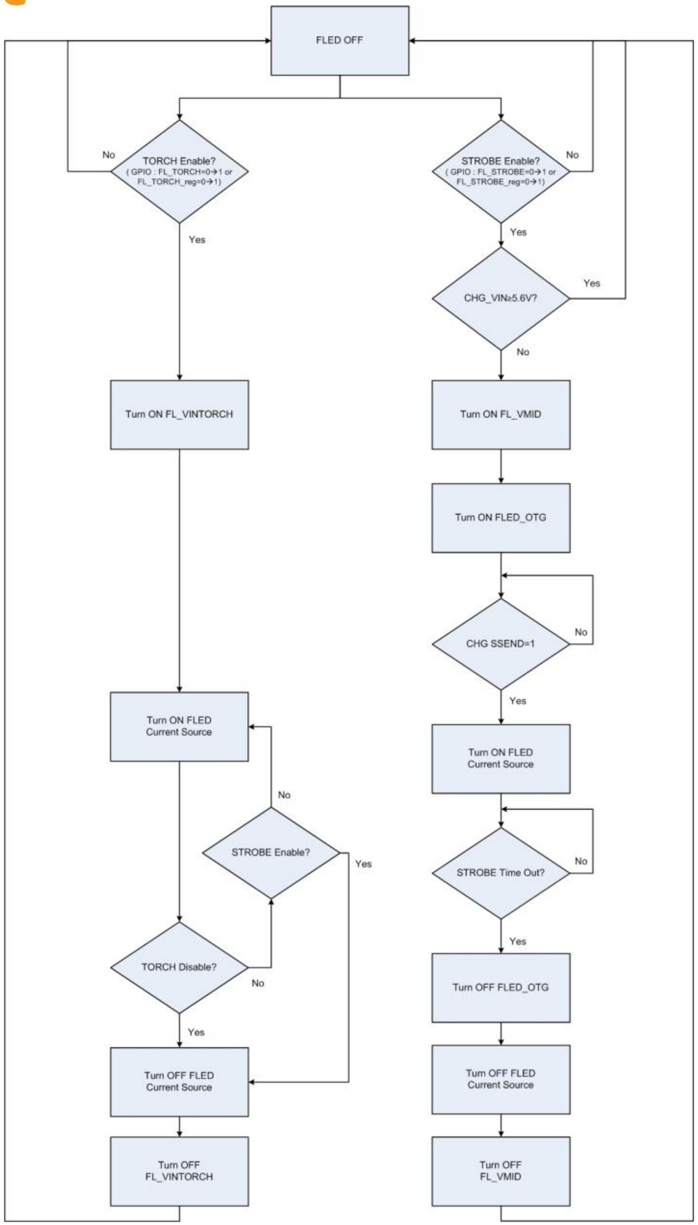
General Function Index

- TOP part
- Charger part
- Flash LED part
- Backlight LED part
- Display Bias part
- RGB part
- LDO part
- PD part

Flow Chart

- Power Source
  - ✓ Torch Mode : Power source auto-selected from FL_VINTORCH
  - ✓ Strobe Mode : Power source auto-selected from FL_VMID
- Protection
  - ✓ Strobe inactivated when CHG_VIN≥5.6V



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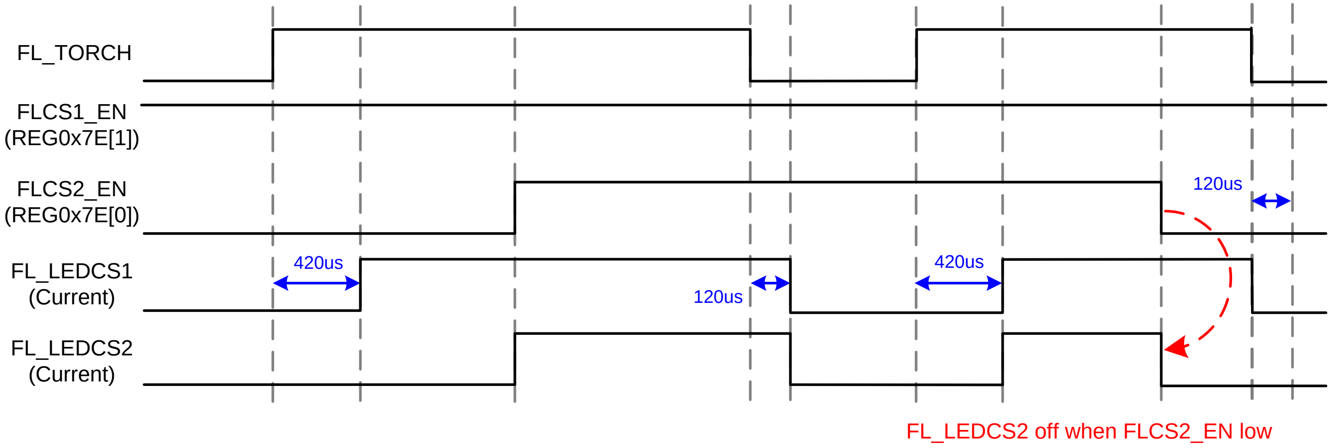
Operation
Torch Mode

- GPIO Control

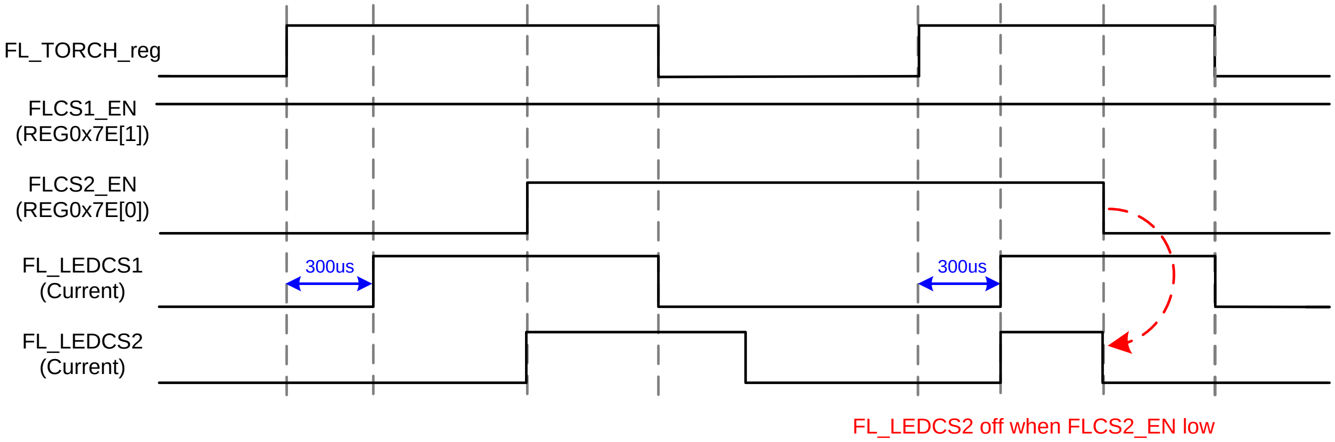
✓ 32 current level (25~400mA)



Note. If FLCS1_EN and FLCS2_EN=0, FLED will not work even FL_TORCH enabled。

- Register Control

✓ 32 current level (25~400mA)



Note. If FLCS1_EN and FLCS2_EN=0, FLED will not work even FL_TORCH_reg is "1"。

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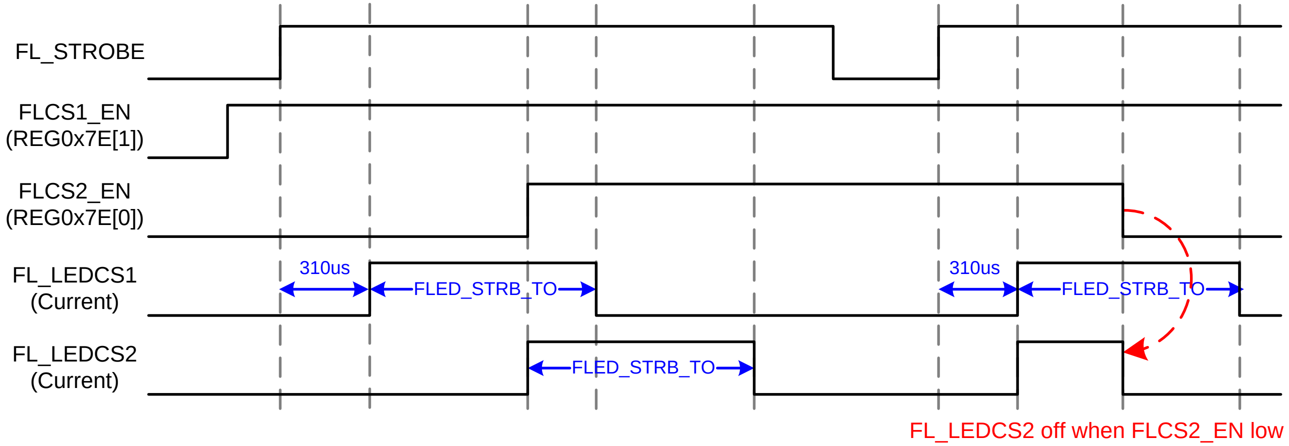
Operation

Strobe Mode

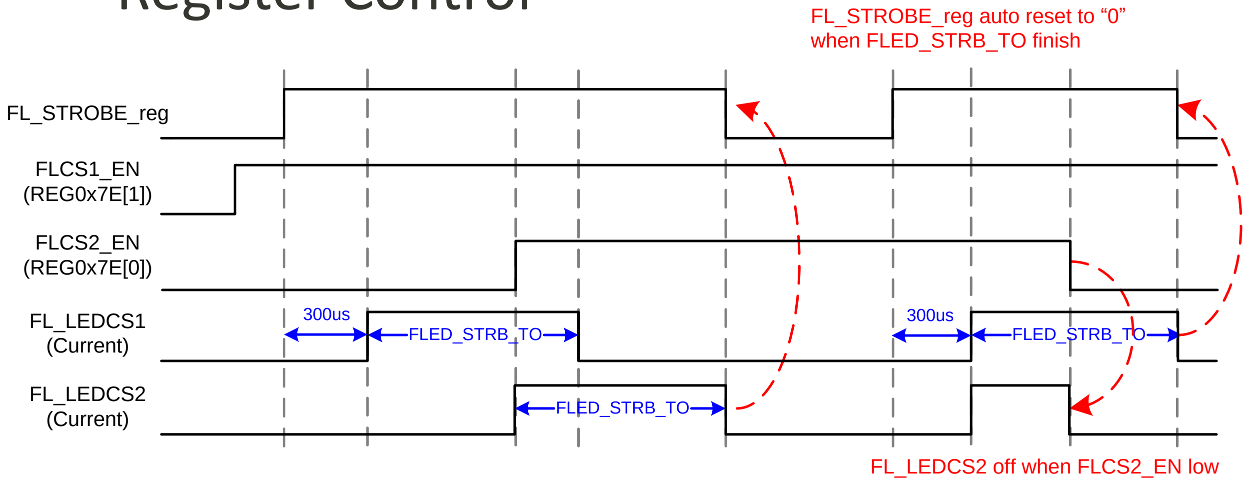
- GPIO Control



- ✓ 128 current level (25~750mA or 50~1500mA)
- ✓ 75 timeout setting (64~2432ms)

Note. If FLCS1_EN and FLCS2_EN=0, FLED will not work even FL_STROBE enabled。

- Register Control



- ✓ 128 current level (25~750mA or 50~1500mA)
- ✓ 75 timeout setting (64~2432ms)
- ✓ FL_STROBE_reg auto-rest to "0" after timeout

Note. If FLCS1_EN and FLCS2_EN=0, FLED will not work even FL_STROBE_reg is"1"。

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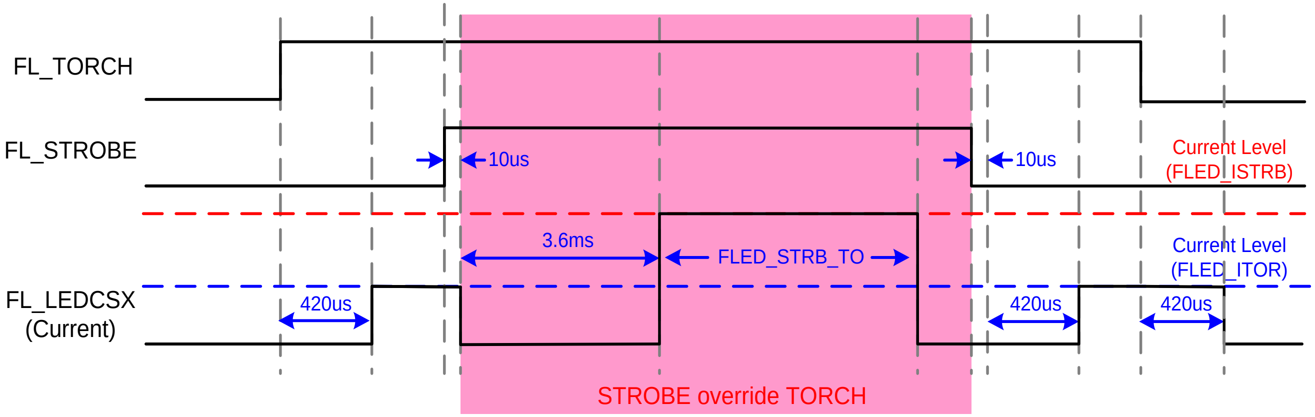
Operation
Strobe/Torch Mode

- GPIO Control

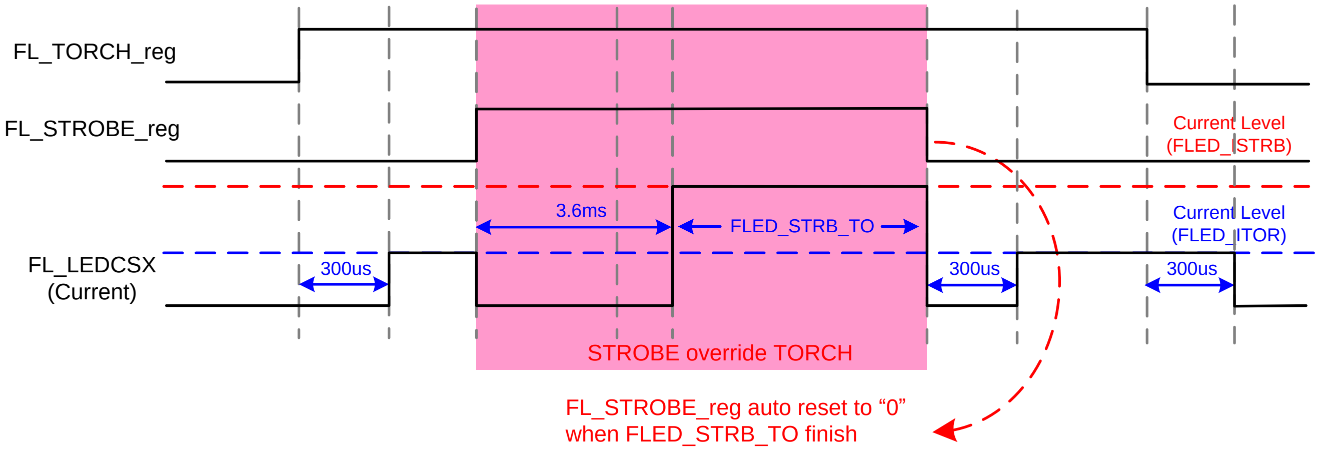


✓ FLED TORCH current suspend and change to STROBE current level when FL_STROBE enables.

✓ FLED change back to TORCH current level after STOBE timeout with suspend time.

Note. If FLCSX_EN=0, FLED will not work even FL_TORCH or FL_STROBE enabled.

- Register Control



✓ FLED TORCH current suspend and change to STROBE current level when FL_STROBE _reg=1.

✓ FLED change back to TORCH current level after STOBE timeout with suspend time.

✓ FL_STROBE_reg is reset to "0" when FLED_STRB_TO finish.

Note. If FLCSX_EN=0, FLED will not work even FL_TORCH or FL_STROBE_reg is"1".

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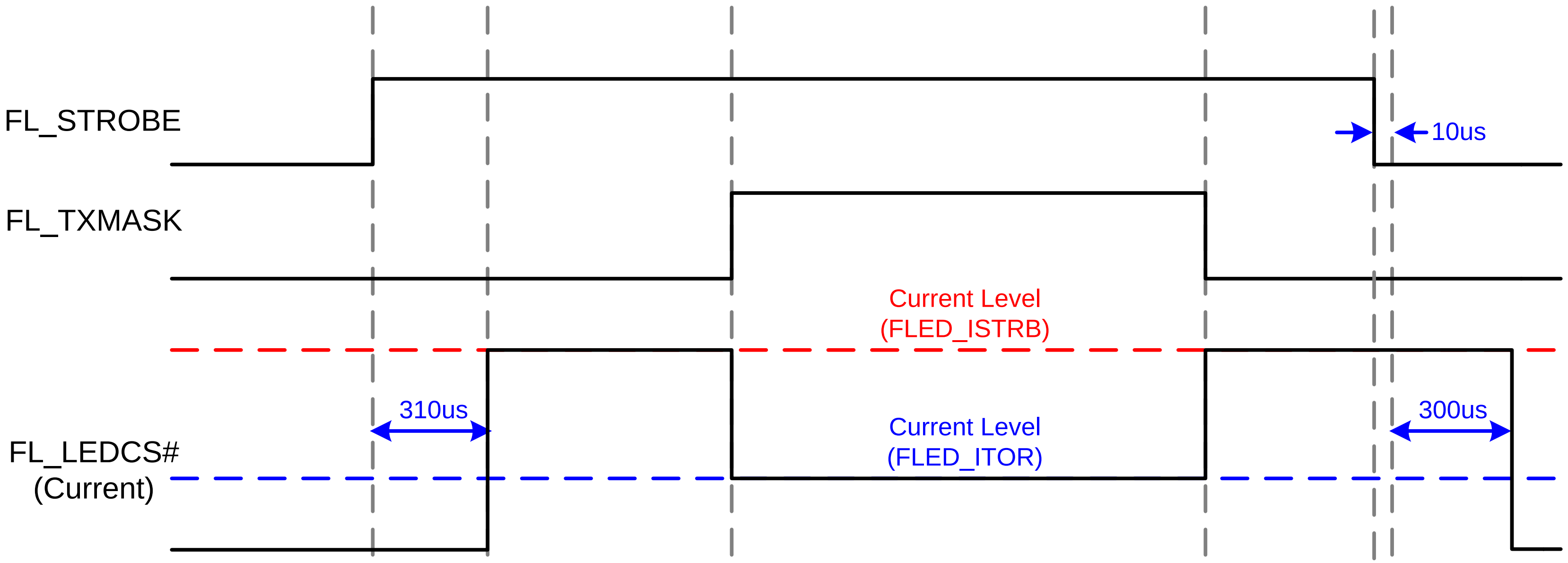
Function Description
Strobe Mode – FL_TXMASK

- TX_ActiveLevel=High Level



✓ TX_ActiveLevel=H, FLED current change to Torch level when FL_TXMASK=H
✓ TX_ActiveLevel=L, FLED current change to Torch level when FL_TXMASK=L

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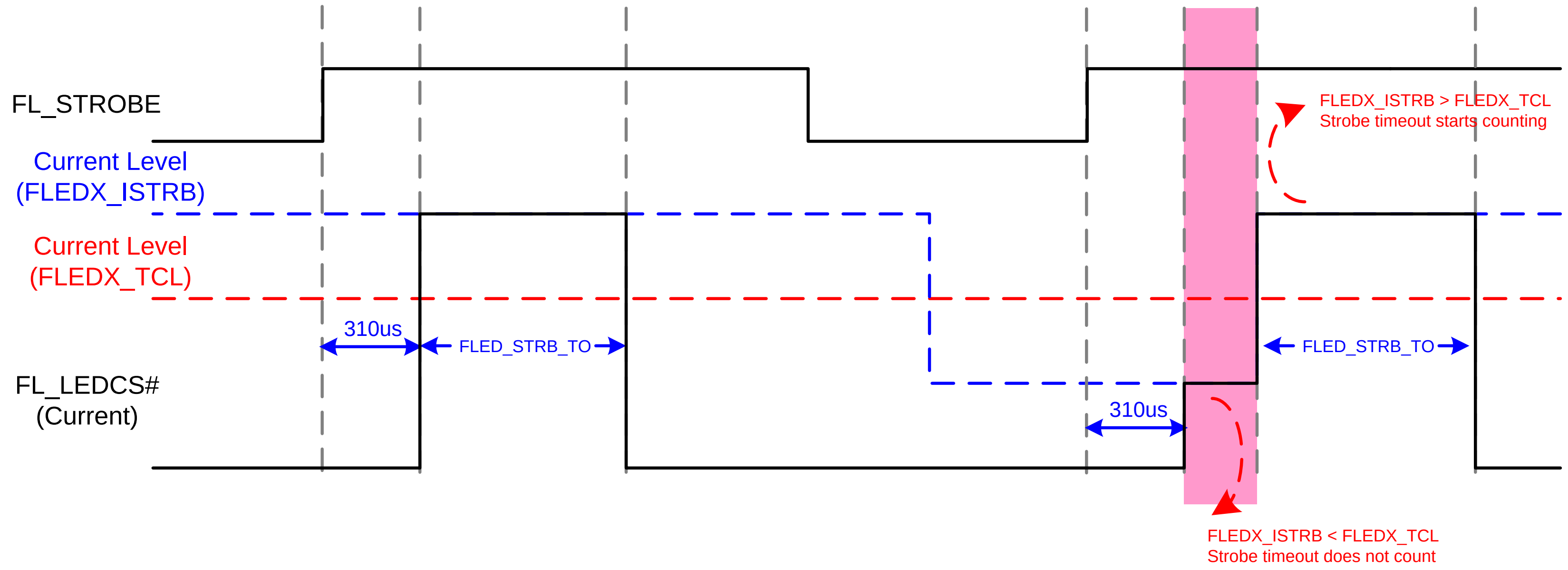
Function Description

Strobe Mode – Timeout Current Level (TCL)



- ✓ Strobe Mode, timeout counts when FLED_ISTRB setting is higher than FLED_TCL.
- ✓ Strobe Mode, timeout does not count when FLED_ISTRB setting is lower than FLED_TCL. It backs to timeout counting after FLED_ISTRB setting is higher than FLED_TCL.

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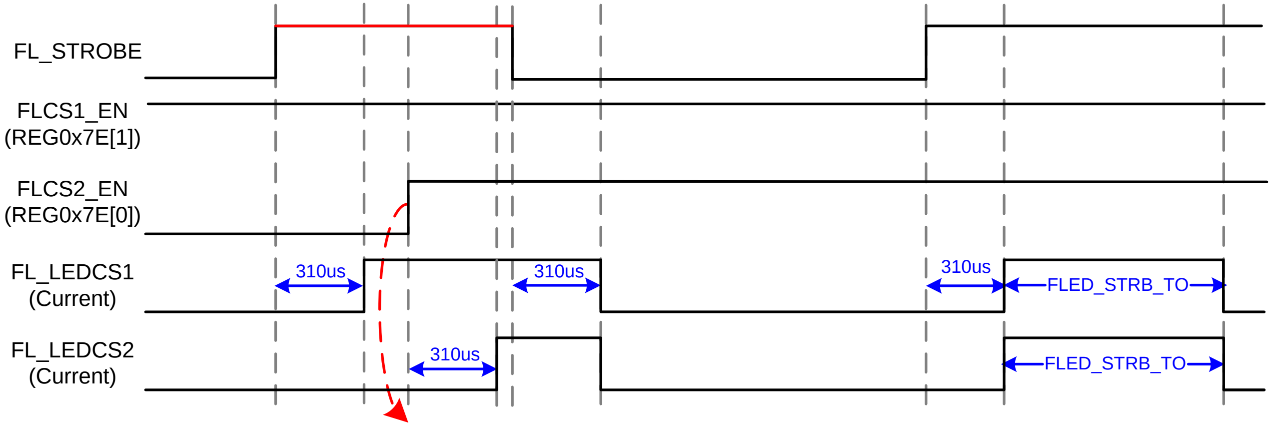
Function Description

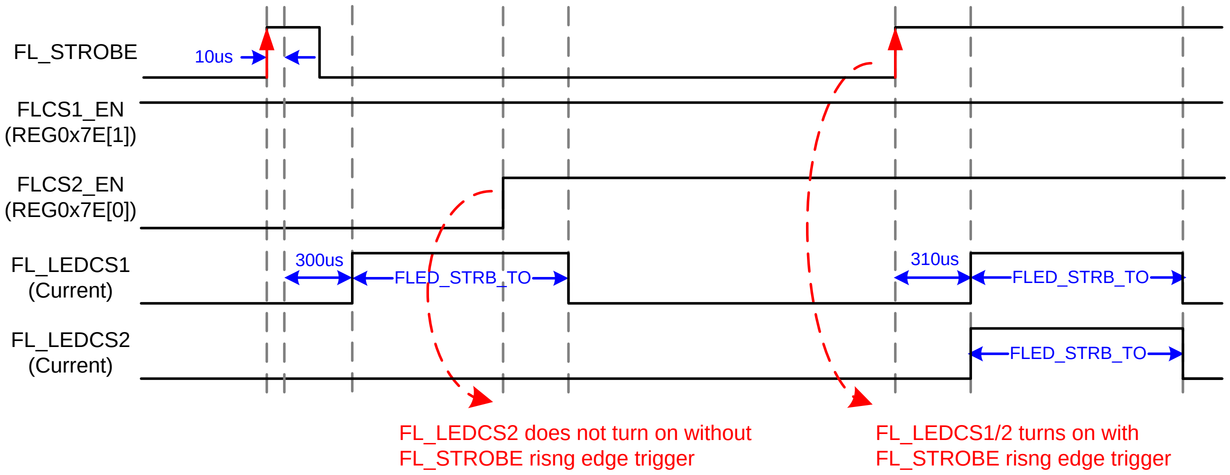
Strobe Mode – GPIO control : Reg0x70[1] FLED_STRB_LES

- Level sensitive



✓ FLED turns on when FLEDCSX_EN and FL_STROBE=1

- Rising edge trigger



✓ FLED turns on when FLEDCSX_EN=1 with FL_STROBE rising edge

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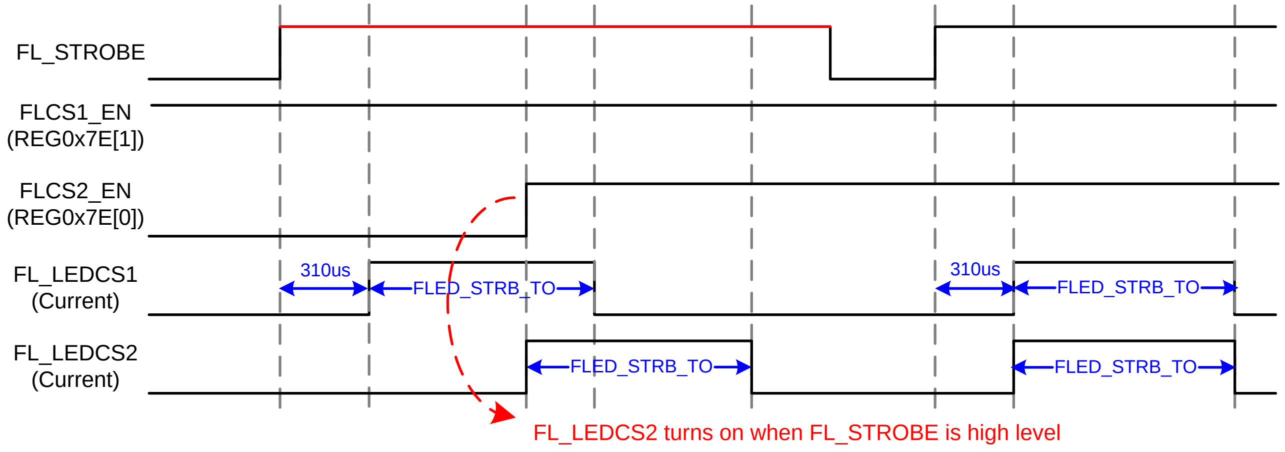
Function Description

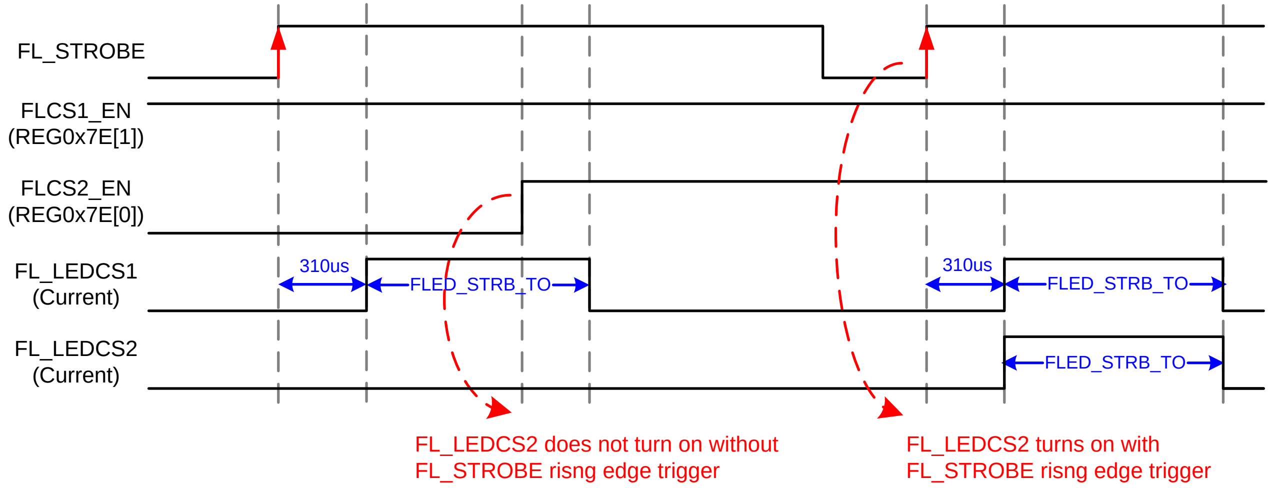
Strobe Mode – GPIO control : Reg0x70[1] FLED_STRB_LES

- Level sensitive



✓ FLED turns on when FLEDCSX_EN and FL_STROBE=1

- Rising edge trigger



✓ FLED turns on when FLEDCSX_EN=1 with FL_STROBE rising edge

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Function Description

Strobe Mode – Supply Limit (High CHG_VIN voltage)

- CHG_VIN over voltage for Strobe function supply limit
  - Strobe function is inactivated when CHG_VIN voltage is higher than 5.6V
  - Strobe function is available when CHG_VIN over voltage condition is removed.

Parameter	Min	Typ.	Max	Units
CHG_VIN OVP Level VIN_OVP_FL	5.45	5.6	5.75	V
Hysteresis VIN_OVP_Hys_FL	0.25	0.3	0.35	V

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Function Description

Short Protection

- FL_LEDCSX voltage for FLED short detection
  - Short condition detected if voltage of FL_LEDCSX is below 1V.(typ.)
  - Output current limited to startup current level(320uA).
  - Interrupt after short condition 2.5ms.(typ.)
  - FLED auto-recovery when short condition is removed.

Parameter	Min	Typ.	Max	Units
Short Detection Level $V_{_SC_FL}$	-	1	1.3	V
Presence Detection Time $T_{D_SC_FL}$	1.8	2.5	3.3	ms

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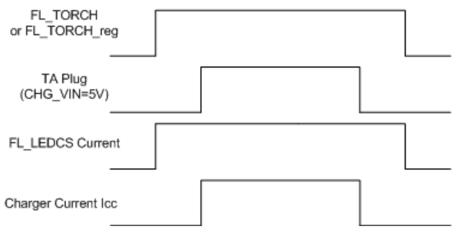
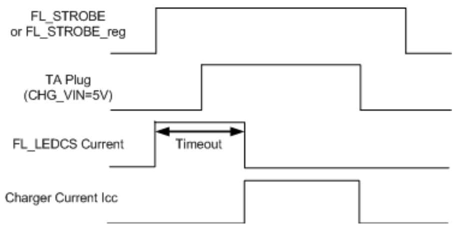
Application

FLED Operation with adapter plug in/out (1)

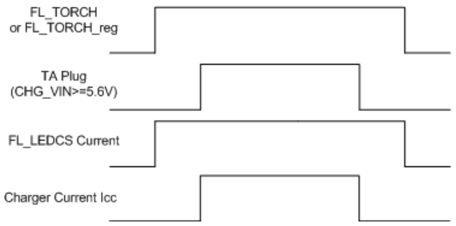
Torch_en→5VTAIn→5VTAOut→Torch_dis



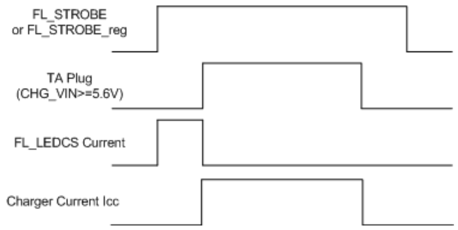
Strobe_en→5VTAIn→5VTAOut→Strobe_dis



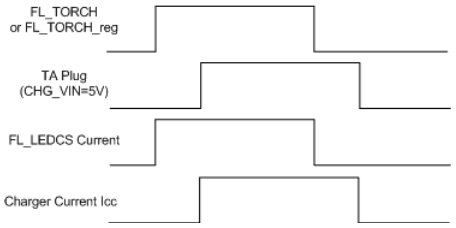
Torch_en→HVTAIn→HVTAOut→Torch_dis



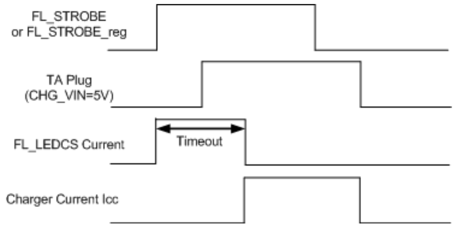
Strobe_en→HVTAIn→HVTAOut→Strobe_dis



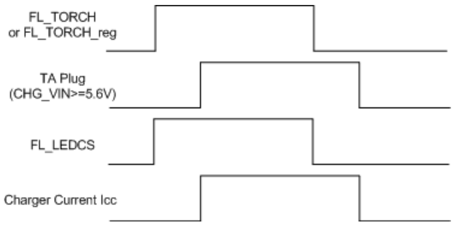
Torch_en→5VTAIn→Torch_dis→5VTAOut



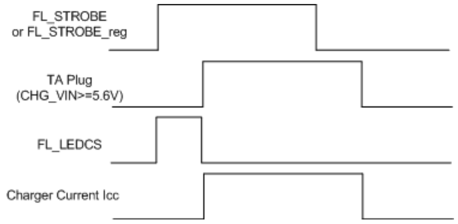
Strobe_en→5VTAIn→Strobe_dis→5VTAOut



Torch_en→HVTAIn→Torch_dis→HVTAOut



Strobe_en→HVTAIn→Strobe_dis→HVTAOut



Note. HVTA with charger voltage ≧5.6V

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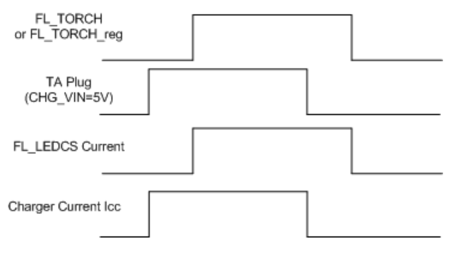
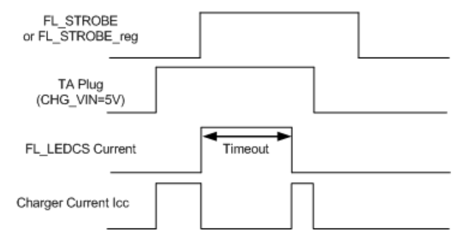
Application

FLED Operation with adapter plug in/out (2)

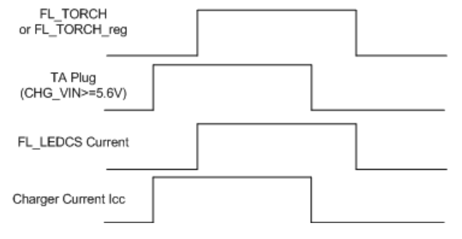
5VTAIn→Torch_en→ 5VTAOut→Torch_dis



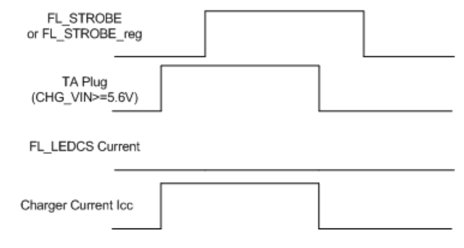
5VTAIn→Strobe_en→ 5VTAOut→Strobe_dis



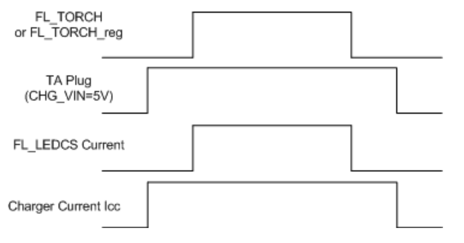
HVTAIn→Torch_en→ HVTAOut→Torch_dis



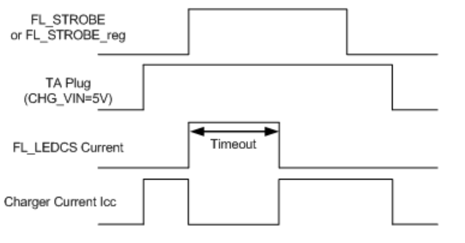
HVTAIn→Strobe_en→ HVTAOut→Strobe_dis



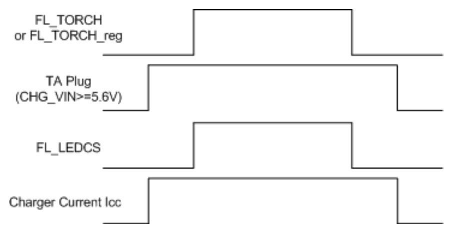
5VTAIn→Torch_en→ Torch_dis→5VTAOut



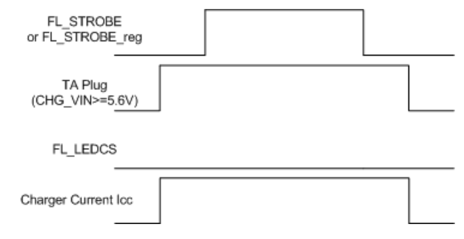
5VTAIn→Strobe_en→ Strobe_dis→5VTAOut



HVTAIn→Torch_en→ Torch_dis→HVTAOut



HVTAIn→Strobe_en→ Strobe_dis→HVTAOut



Note. HVTA with charger voltage ≧5.6V

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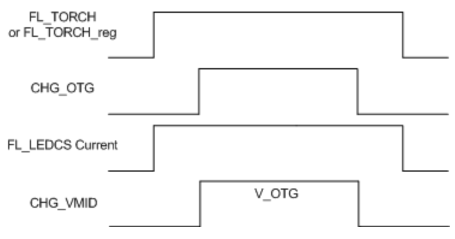
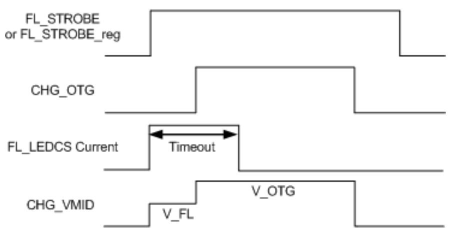
Application

FLED Operation with OTG

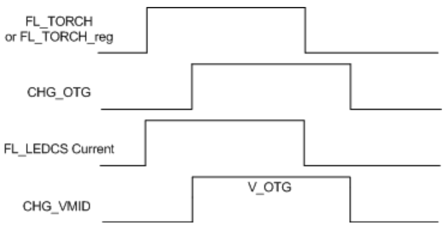
Torch_en→OTGOn→OTGOff→Torch_dis



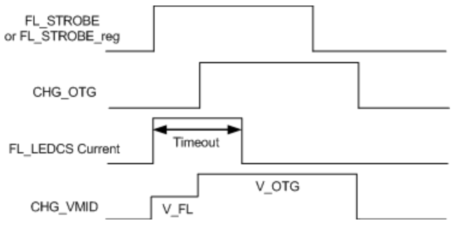
Strobe_en→OTGOn→OTGOff→Strobe_dis



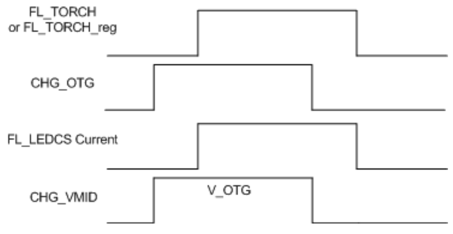
Torch_en→OTGOn→Torch_dis→OTGOff



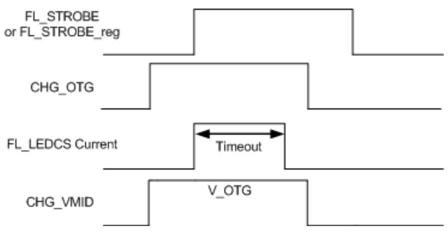
Strobe_en→OTGOn→Strobe_dis→OTGOff



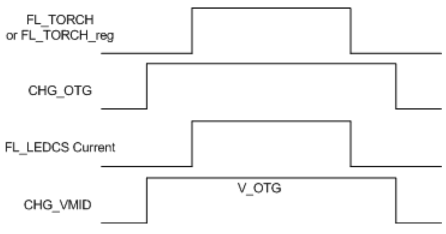
OTGOn→Torch_en→OTGOff→Torch_dis



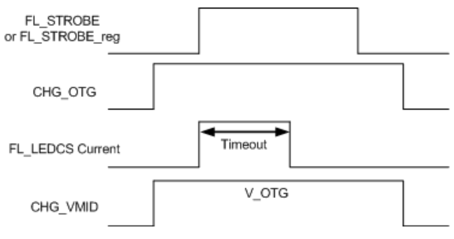
OTGOn→Strobe_en→OTGOff→Strobe_dis



OTGOn→Torch_en→Torch_dis→OTGff



OTGOn→Strobe_en→Strobe_dis→OTGff



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General Function Index

- TOP part
- Charger part
- Flash LED part
- Backlight LED part
- Display Bias part
- RGB part
- LDO part
- PD part

Backlight Operation
BL Mode

BL_EN 0xA0[6]	BL_ENx 0xA0 [5:2]	BL_PWM 0xA2[7]	PWM pin	Status
0	X	X	X	Standby
1	0000	X	X	LED Bias enable
1	1111	0	X	ILEDx= BLED Brightness
1	1111	1	0	LED Bias enable
1	0000	1	Duty	LED Bias enable
1	1111	1	Duty	ILEDx=(BLED Brightness*PWM Duty)

The normal LCD panel power sequence timing is that enable DSV function at first then enable Backlight function.

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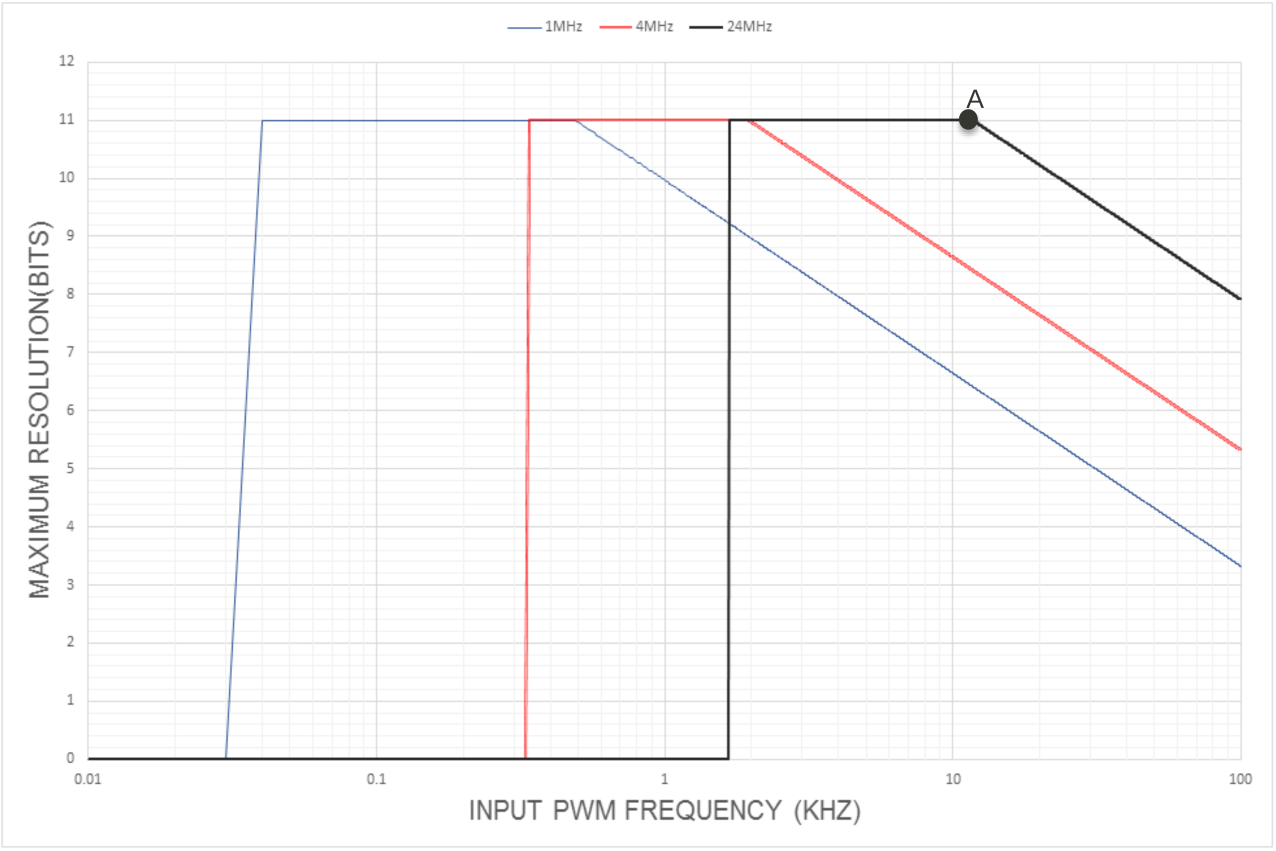
PWM dimming resolution select

- ✓ To achieve the full 11-bit maximum resolution of PWM duty cycle to the LED brightness code, the input PWM duty cycle must be ≥ 11 bits, and the PWM sample period (1/ƒSAMPLE) must be smaller than the minimum PWM input pulse width. The PWM_fsample could be selected by 0xA2[4:3]. Below shows the ideal maximum resolutions based on the input PWM frequency. The minimum PWM frequency for each PWM sample rate is based on PWM timeout.

0xA2[4:3]	PWM_fsample
00	1MHz
01	4MHz
1X	24MHz

Note: The maximum of PWM dimming frequency which can achieve the full 11bit resolution is 11KHz (Point A)



PWM dimming TimeOut & Auto Frequency

- ✓ The PWM timeout feature turns off the boost output when the PWM is enabled and there is no PWM pulse detected. The timeout duration changes based on the PWM Sample Rate selected which results in a minimum supported PWM input frequency. The sample rate, timeout, and minimum supported PWM frequency are summarized in below table.

SAMPLE RATE	TIMEOUT	MINIMUM SUPPORTED PWM FREQUENCY
1MHz	25ms	40Hz
4MHz	3ms	333Hz
24MHz	0.6ms	1.66kHz

PWM Timeout and Minimum Supported PWM Frequency vs PWM Sample Rate

- ✓ When bled_dim code is equal to or less than the bled_autofrequency, the backlight boost switching frequency is set to 500kHz. It can improve the efficiency with fine-tune the auto frequency value.

Auto Switching Frequency code	SWITCHING FREQUENCY
< Auto Frequency select (register 0xA6[7:0])	500kHz
>Auto Frequency select (register 0xA6[7:0])	1MHz

Auto Switching Frequency Operation

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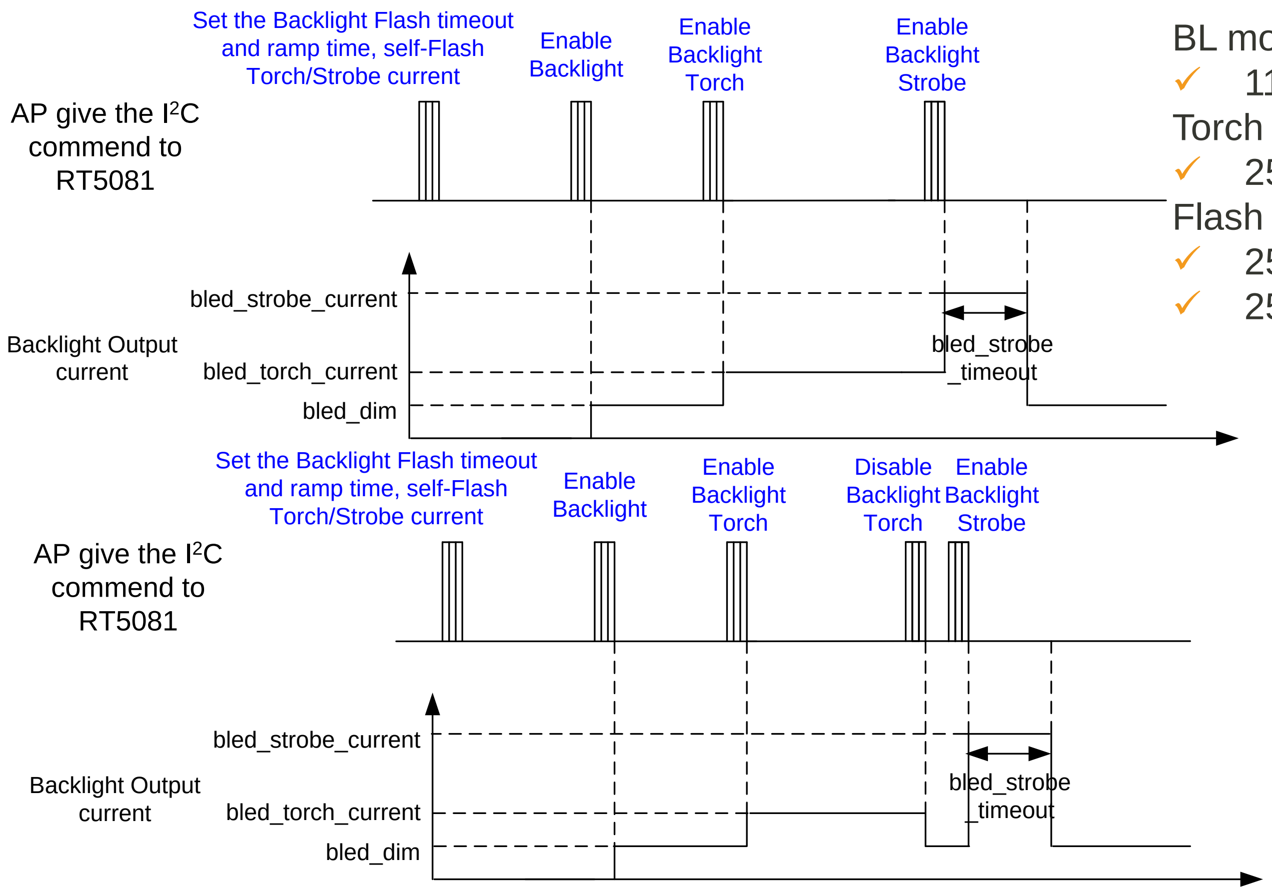
Mode Operation

It suggest that setting the self Flash by below illustration.



BL mode
- ✓ 11 bit resolution

Torch mode
- ✓ 256 step current level (0mA~30mA)

Flash mode
- ✓ 256 step current level (0mA~30mA)
- ✓ 256 step timeout setting (16~2048ms)

- ✓ The mode change is suggest that finish the previous mode current target then change to next mode.(Torch/Strobe/Backlight)

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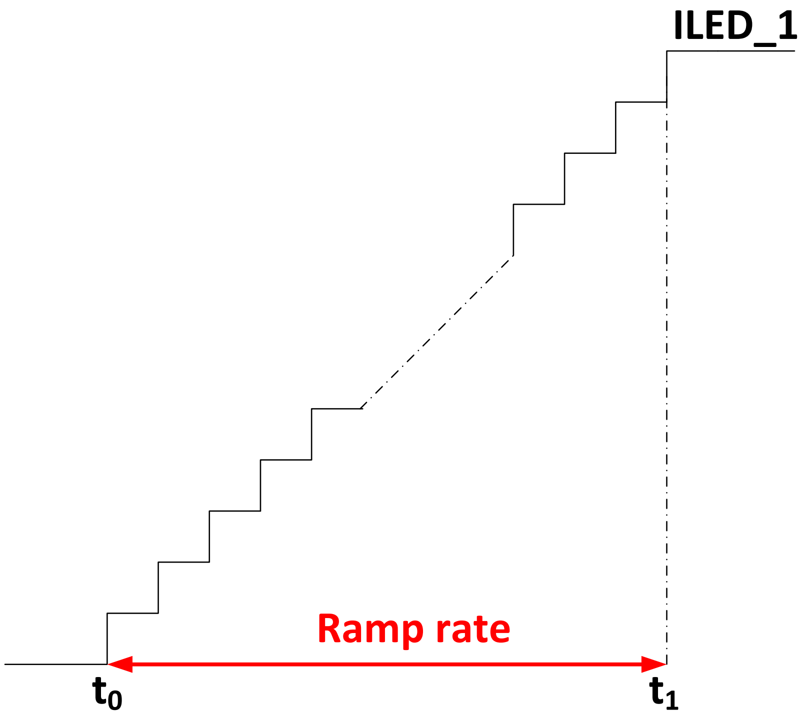
Ramp time for ramp up/down



BL mode

- ✓ Setting 0xA3 [7:4]
- ✓ 16 ramp time level (0~8s)

Flash mode

- ✓ Setting 0xA7 [5:3]
- ✓ 6 ramp time level (0~5ms)

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Recommend operation for heavy load

- The RT5081 has 4 selectable OCP levels.(0.9A,1.2A,1.5A,1.8A).
- The inductor current peak is related to VSYS range, frequency and loading.

  When using 8s4p LEDs for the max current 30mA/per string(Iout=120mA) by 1MHz switching frequency, the VSYS >3.6V can avoid trigger OCP.

Recommend inductor	MDMK4040T-100MM	DFE322512-100M

- Recommend operation for heavy load:

OCP:+/-20%@1.8A, LED:8s4p ,30mA/per string (Iout=120mA),VF=3.3V bled_ramptime≥500us		
VSYS operation range(V)	**L(uH)** @+/-20%	**Frequency(Hz)** @+/-10%
>3.6V	10	1M
>3.8V	10	500k

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DB enable control

db_ext_en 0xB0[0]	DB_ENP	DB_ENN	db_vpos_en 0xB1[6]	db_vneg_en 0xB1[3]	Status
0	X	X	0	0	Standby
0	X	X	1	0	POSVOUT enable
0	X	X	0	1	NEGVOUT enable
0	X	X	1	1	POSVOUT & NEGVOUT enable
1	0	0	X	X	Standby
1	1	0	X	X	POSVOUT enable
1	0	1	X	X	NEGVOUT enable
1	1	1	X	X	POSVOUT & NEGVOUT enable

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DB operation setting

Channel	Range	Step	Register	Default Value
BSTVOUT	4V~6.15V	50mV/LSB	0xB2[5:0]	5.7V
POSVOUT	4V~6V	50mV/LSB	0xB3[5:0]	5.5V
NEGVOUT	-4V~-6V	50mV/LSB	0xB4[5:0]	-5.5V

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DB single control

db_ext_en 0xB0[0]	db_signal_pin 0xB0[5]	DB_ENP	DB_ENN	Status
1	0	0	0	Standby
1	0	1	0	POSVOUT enable
1	0	0	1	NEGVOUT enable
1	0	1	1	POSVOUT & NEGVOUT enable
1	1	0	X	Standby
1	1	1	X	POSVOUT & NEGVOUT enable

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DB delay time control

0xB2[7:6]	Delay time	Power on	Power off
00	No constraint	POSVOUT start to ramp up when DB_ENP=H or db_vpos_en =1 NEGVOUT start to ramp down when DB_ENN=H or db_vneg_en=1	NEGVOUT start to discharge when DB_ENN=L or db_vneg_en=0 POSVOUT start to discharge when DB_ENP=L or db_vpos_en=0
01	0ms	POSVOUT start to ramp up when DB_ENP=H or db_vpos_en=1 NEGVOUT start to ramp down after POSVOUT ramp up to target and delay 0ms even the DB_ENN=H or db_vneg_en=1	NEGVOUT start to discharge when DB_ENN=L or db_vneg_en=0 POSVOUT start to discharge after NEGVOUT discharge to GND and delay 0ms even the DB_ENP=L or db_vpos_en=0
10	1ms	POSVOUT start to ramp up when DB_ENP=H or db_vpos_en=1 NEGVOUT start to ramp down after POSVOUT ramp up to target and delay 1ms even the DB_ENN=H or db_vneg_en=1	NEGVOUT start to discharge to GND when DB_ENN=L or db_vneg_en=0 POSVOUT start to discharge after NEGVOUT discharge to GND and delay 1ms even the DB_ENP=L or db_vpos_en=0
11	4ms	POSVOUT start to ramp up when DB_ENP=H or db_vpos_en=1 NEGVOUT start to ramp down after POSVOUT ramp up to target and delay 4ms even the DB_ENN=H or db_vneg_en=1	NEGVOUT start to discharge when DB_ENN=L or db_vneg_en=0 POSVOUT start to discharge after NEGVOUT discharge to GND and delay 4ms even the DB_ENP=L or db_vpos_en=0

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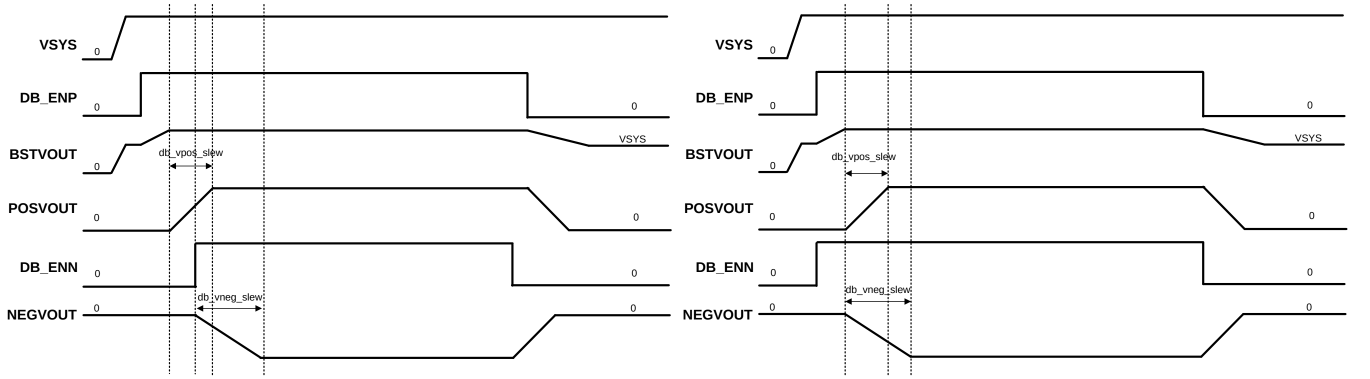
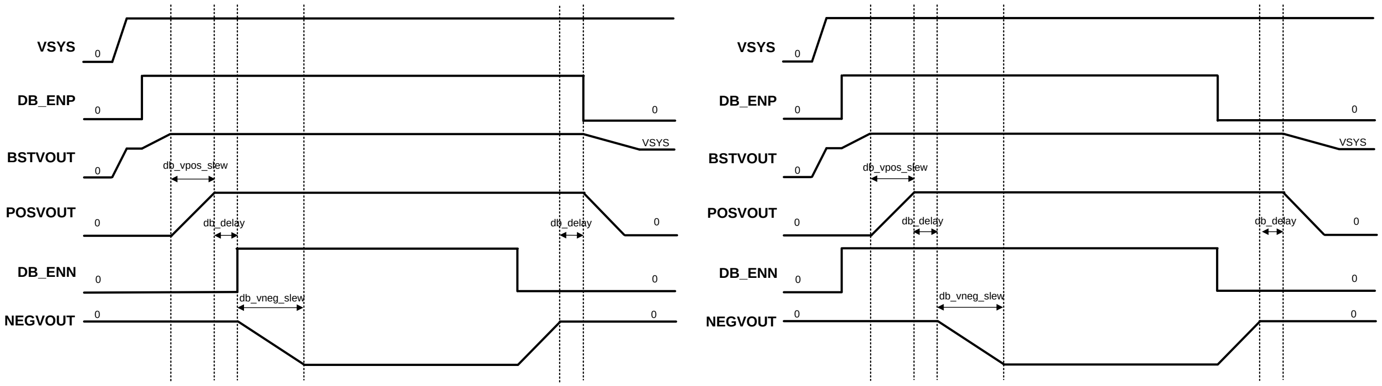
DB power sequence

- DB delay no constraint



- DB delay



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Power saving mode

- Power saving mode to bypass the input voltage to POSVOUT and NEGVOUT. Enable the 0xB1[7]=1 to control the high side switch of boost converter and the LDO fully turn on to save the quiescent current and switching current. The POSVOUT=Vin and NEGVOUT=-Vin.

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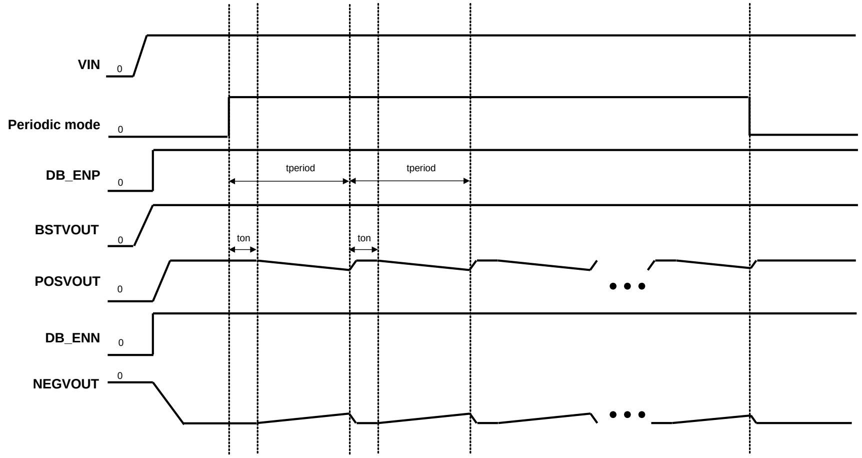
DB periodic mode

- The RT5081 supports the DB periodic mode with the enable bit 0xB0[7] and frequency select bit 0xB0[6]. In the periodic mode, the enabled channel of the POSVOUT and NEGVOUT will repeat on/off sequence. The delay time, slew rate, discharge and GND connect follow the register setting.

db_periodic_mode 0xB0[7]	db_freq_pm 0xB0[6]	ton (ms)	tperiod (ms)
0	0	X	X
0	1	X	X
1	0	2	50
1	1	1.6	30



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Discharge mode

- The RT5081 provides internal switch resister to discharge the output voltage during the channel power off. Setting register 0xB1[4]=1 and 0xB1[1]=1 to enable the discharge function of POSVOUT and NEGVOUT individually. The output will keep connecting to GND when the register 0xB1[5]=1 and 0xB1[2]=1.

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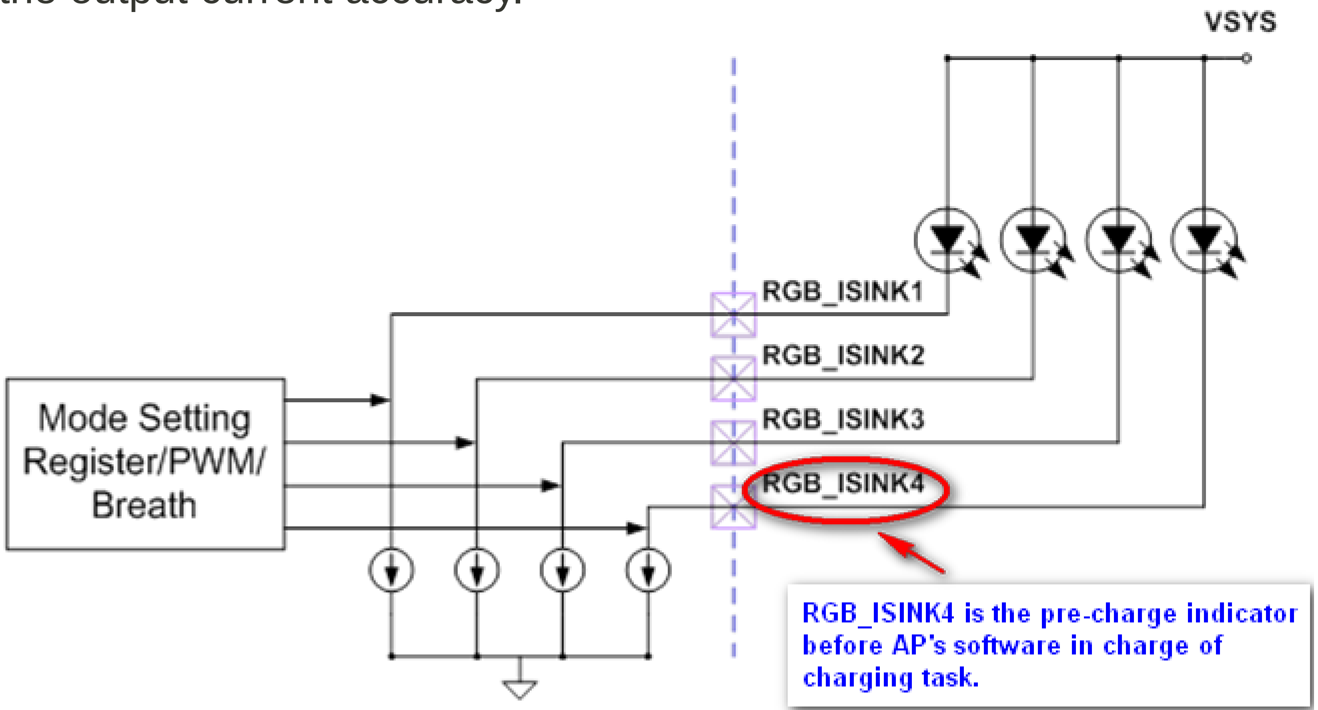
- PD part

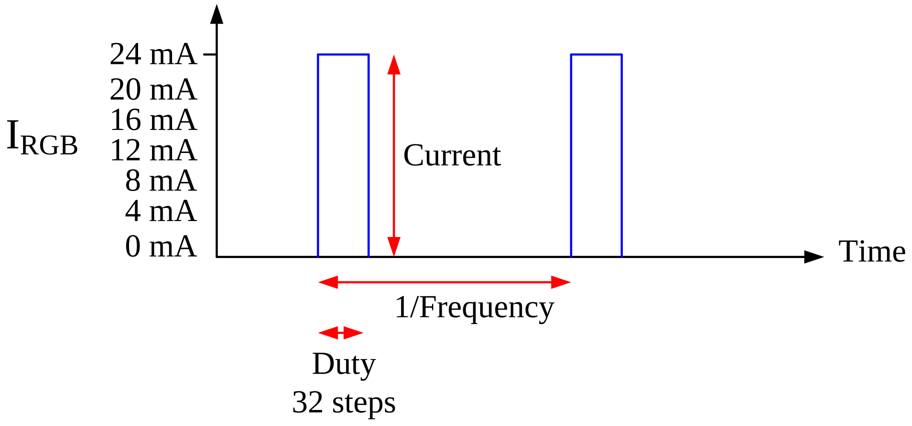
RGB application circuit

- It is a four-channel LED driver designed to produce variety of lighting effects for mobile device. The device is gradually increase or decrease the brightness of the backlight LED upon command by I^2C control, and it also can support RGB mode to select PWM mode, breath mode and Register mode.
- The RGB_ISINK4 default setting is auto mode that using for TA charging indicator, It also support to software mode by 0x85[4] (Can be programmable as RGB_ISINK1~RGB_ISINK3).
- For the RGB application, user must consider the LED forward voltage, the RT5081 RGB current sink headroom and the minimum battery application voltage to make sure the output current accuracy.



RGB PWM mode

- The RT5081 features a built-in PWM mode control by setting ISINKx_DIM_MODE to 00. The RGB_ISINK1~RGB_ISINK3 of the RT5081 can provide up to 24 mA per string. There are 7 step LED current control by setting ISINKx_CUR_SEL each channel. The ON/OFF of the current source is synchronized to the PWM signal. The frequency of LED current is equal to the PWM input signal that is setting by ISINKx_DIM_FSEL. In order to guarantee the PWM resolution, the PWM frequency have to be operated at range of 0.1Hz to 1kHz that is selected by ISINKx_DIM_FSEL.



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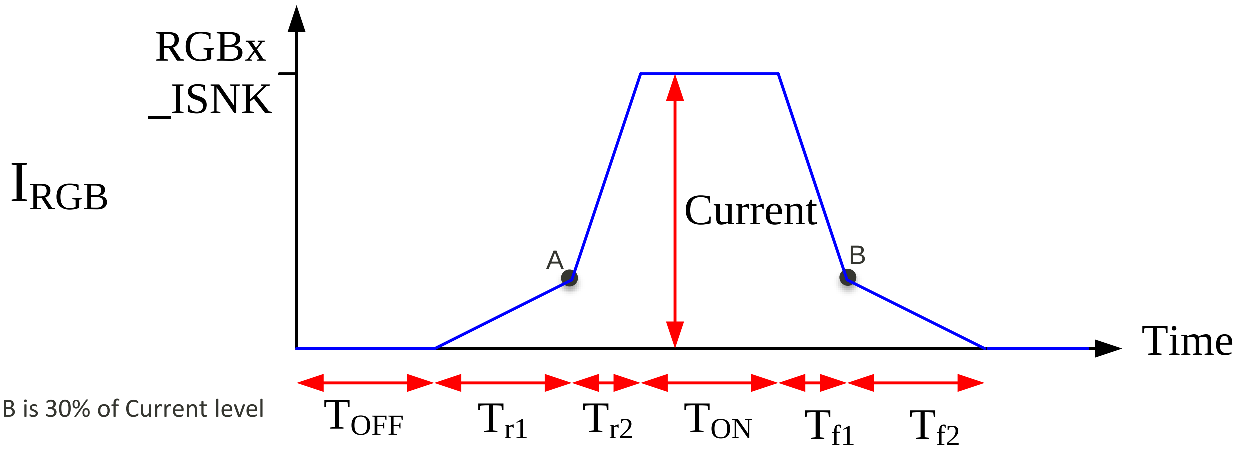
RGB Breath mode

- In the breath mode, the 3 channels of the RT5081 can provide up to 24 mA per string. There are 7 step LED current control by setting register ISINKx_CUR_SEL each channel.
- In order to provide a smooth breath mode, there are 6 period timing to control the rising time and falling time, and it is control by setting register ISINKx_VREATH_TON_SEL, ISINKx_BREATH_TOFF_SEL, ISINKx_BREATH_Trx_SEL and ISINKx_BREATH_Tfx_SEL.



Note: The IRGB of point A & B is 30% of Current level

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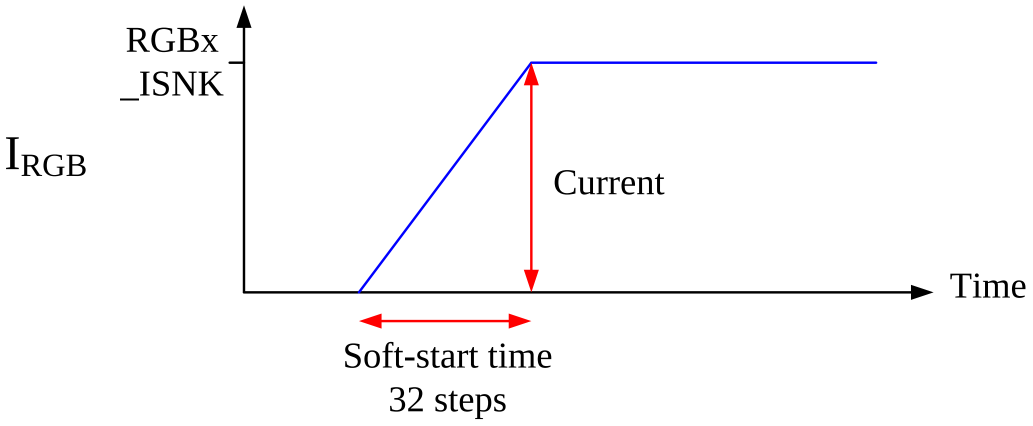
RGB Register mode

- The RT5081 features a built-in register mode control by setting ISINKx_DIM_MODE to 1X. The register ISINKx_SFSTR_EN control the soft-start time ON/OFF. If ISINKx_SFSTR_EN is enable, ISINKx_SFSTRx_TC can select soft start time for the each step. The four channels of the RT5081 can provide up to 24 mA per string. There are 7 step LED current control by setting register ISINKx_CUR_SEL each channel.



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General Function Index

- TOP part
- Charger part
- Flash LED part
- Backlight LED part
- Display Bias part
- RGB part
- LDO part
- PD part

General Description

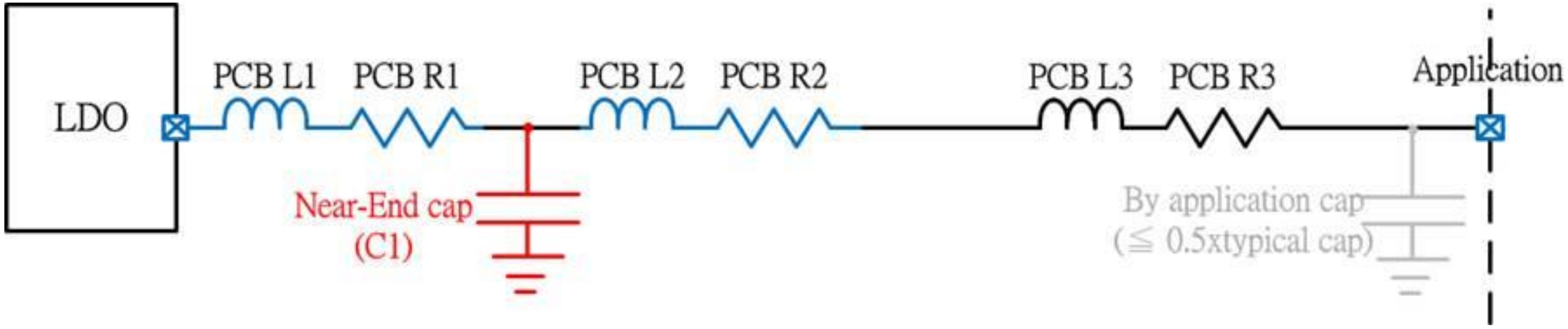
- The output voltage is programmable in the range of 1.6V to 4V via the I^2C interface.

C_{IN} and C_{OUT} Selection

- **C_{IN} :Use a capacitor which value is greater than 2.2µF on the LDO input** and the amount of capacitance can be increased without limit.
- **C_{OUT} : Use a ceramic capacitor which value is at least 2.2µF and its ESR should be within 1mΩ ~ 10mΩ** on the LDO output to make it's stable.

Normal #1 LDO Layout Constraints

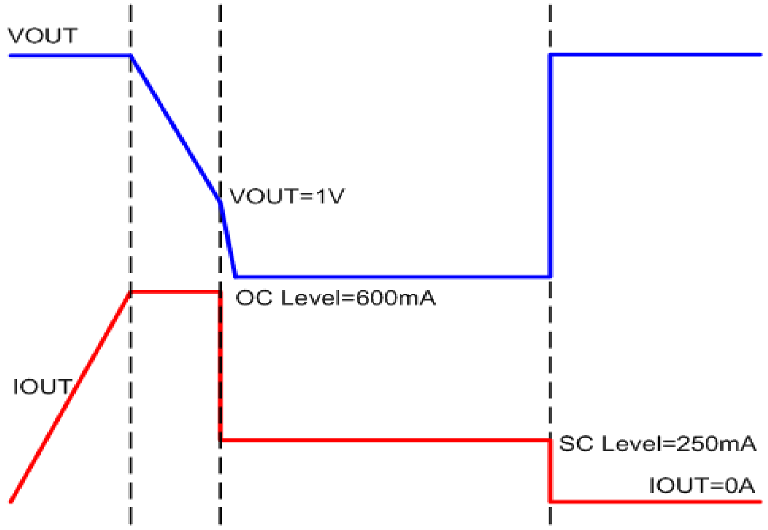
LDO Type	R1 (Trace resistance)	L1 (Trace inductance)	R1+R2 (Trace resistance)	L1+L2 (Trace inductance)	R1+R2+R3 (Trace resistance)	L1+L2+L3 (Trace inductance)
Normal #1	≦0.05 Ω	≦3 nH	X	X	X	X
Normal #2	≦0.05 Ω	≦2 nH	X	X	≦0.05 Ω	≦6 nH



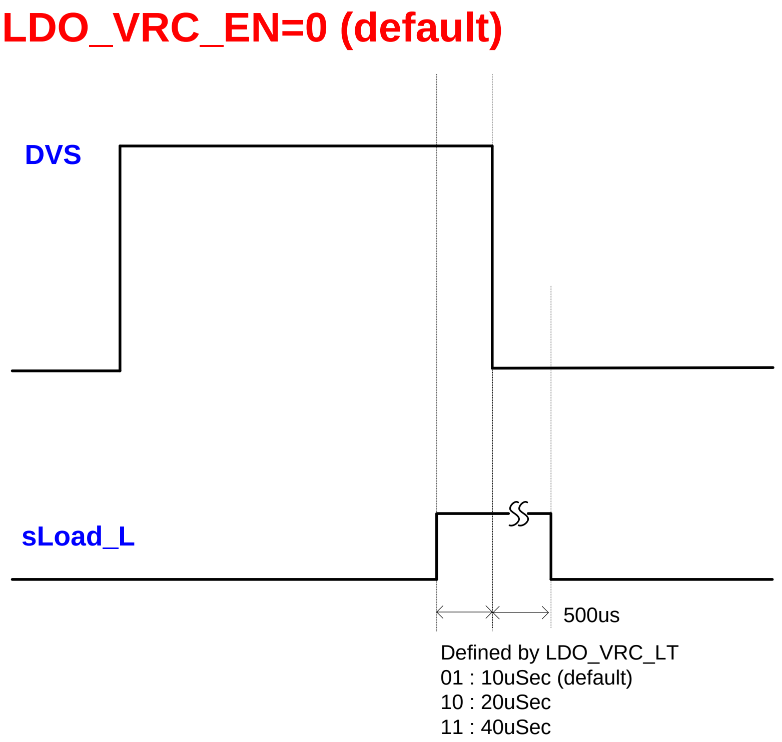
Current Limit

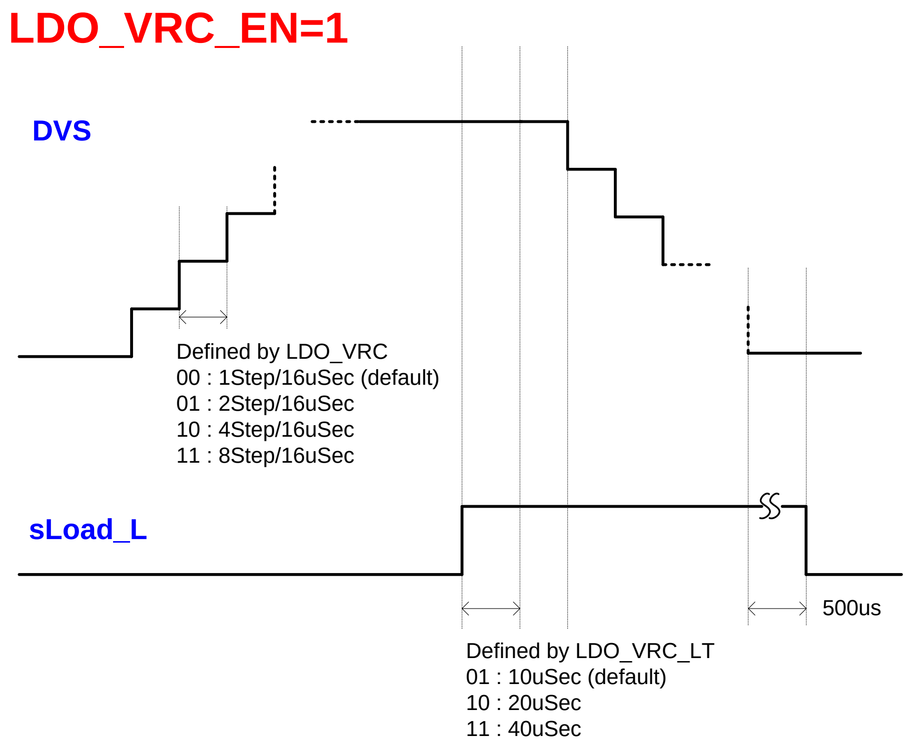
- The LDO monitors and controls the PMOS' gate voltage, **minimum limiting the output current to 600mA.** When the **Vout falls below 1V,** the current limit level falls to **250 mA**. As the loading < 250mA , Vout recover to normal setting value immediately. The output can be shorted to ground for an indefinite period of time without damaging the part.

	Protection Type	Threshold (Typical Value)	Delay Time	Protection Method	Reset Method
LDO	Current Limit	OC level=600mA, Vout > 1V SC level=250mA, Vout ≦ 1V	0s	Vout goes low.	Hiccup



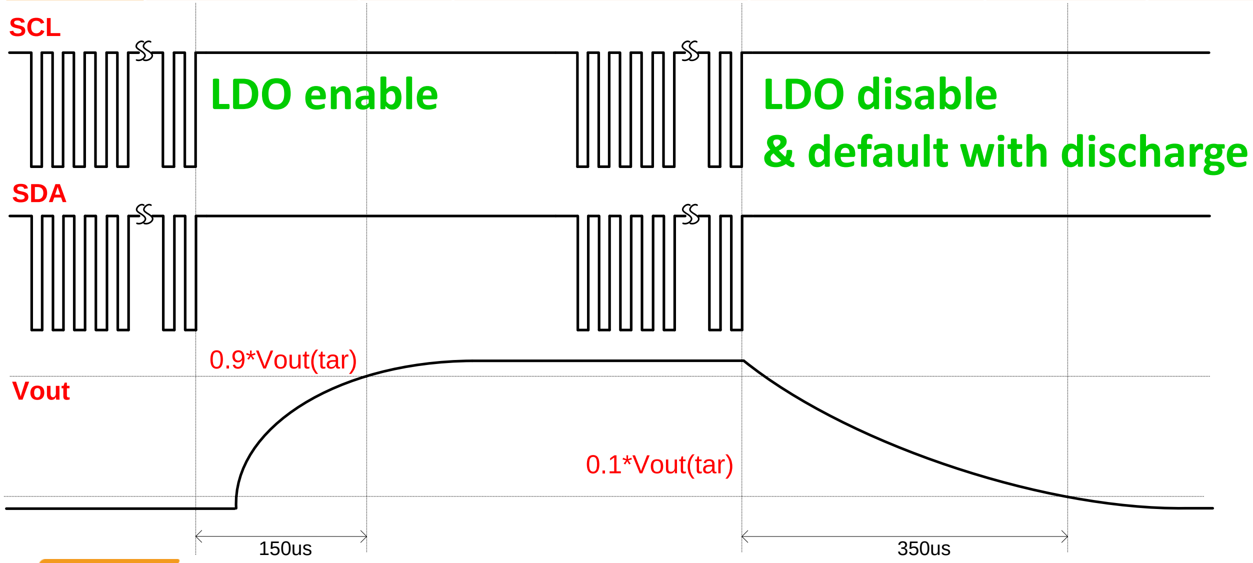
LDO_CFG


LDO_VRC_EN=0 (default)
DVS
sLoad_L
500us
Defined by LDO_VRC_LT
01 : 10uSec (default)
10 : 20uSec
11 : 40uSec


LDO_VRC_EN=1
DVS
Defined by LDO_VRC
00 : 1Step/16uSec (default)
01 : 2Step/16uSec
10 : 4Step/16uSec
11 : 8Step/16uSec
sLoad_L
500us
Defined by LDO_VRC_LT
01 : 10uSec (default)
10 : 20uSec
11 : 40uSec

Power on/off sequence

Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x81	LDO_VOUT (General LDO Output)	7	LDO_EN	0	RW	LDO Enable 0 : Disable 1 : Enable
		6:4	Reserved	000	RW	Keep default value
		3:0	LDO_VOUT	1001	RW	LDO output voltage regulation, 200mV per Step. 0000 : 1.6V 0001 : 1.8V 0010 : 2.0V ... 1000 : 3.2V 1001 : 3.4V ... 11XX : 4.0V



General Function Index

- TOP part
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- Backlight LED part
- Display Bias part
- RGB part
- LDO part
- PD part

Content

PD function of RT5081 follows USB Type-C Port Controller Interface spec 1.0. Some “Not support” functions are listed in the register table.
The following functions are not standard functions defined in TCPC spec.

1. PD Interrupt Reset Function
2. PD Watch Dog Function
3. PD I^2C Reset Function
4. PD Power Mode

PD Interrupt Reset Function

Addr	Bit	BitName	Default	Type	Description
0x9C	7	**INT_RST_EN**	0	RW	1: Enable the INT timeout reset. 0: Disable the INT timeout reset.
0x9C	1:0	**INT_RST_SEL**	01	RW	INT timeout time = (INT_RST_SEL+1) * 0.2 sec

0x9C[7]=1b:
As PD_IRQB is low and AP does not clear alarm status, RT5081 will soft-reset PD function after PD_IRQB low by INT timeout time (0x9C[1:0].)

0x9C[7]=0b:
RT5081 will not soft-reset PD function automatically while PD_IRQB is low for INT timeout time (0x9C[1:0].)

PD Watch Dog Function

Addr	Bit	BitName	Default	Type	Description
0x9D	7	**WATCHDOG_EN**	0	RW	1: Enable the watchdog. 0: Disable the watchdog.
0x9D	2:0	**WATCHDOG_SEL**	100	RW	watchdog timeout time = (WATCHDOG_SEL+1) * 0.4 sec
0x98	2	**INT_WATCHDOG**	0	RW	1b: Watchdog timeout is coming.
0x99	2	**M_WATCHDOG**	0	RW	0b: Interrupt masked, 1b: Interrupt unmasked

0x9D[7]=1b:
0x98[2] will be 1b after 0x9D[7]=1b by watchdog timeout time (0x9D[2:0].)

0x9D[7]=0b:
Disable PD Watch Dog Function.

0x99[2]=1b:
While 0x98[2]=1b, PD_IRQB will be low.

0x99[2]=0b:
While 0x98[2]=1b, PD_IRQB will not be low.

0x98[2]=1b:
0x98[2] will be 1b after 0x9D[7]=1b by watchdog timeout time (0x9D[2:0]). Writing this bit as “1” to clear this bit.

0x98[2]=0b:
PD Watch Dog event does not yet happen.

PD I2C Reset Function

Addr	Bit	BitName	Default	Type	Description
0x9E	7	**I2C_TO_RST_EN**	0	RW	1: Enable the I2C timeout reset function. (SCL and SDA keep low)
0x9E	3:0	**I2C_TO_RST_SEL**	1000	RW	timeout time = (I2C_TO_RST_SEL+1) * 12.5ms

0x9E[7]=1b:
SCL and SDA are low for the timeout time (0x9E[3:0].) RT5081 will soft-reset PD function.

0x9E[7]=0b:
RT5081 will not soft-reset PD function automatically while SCL and SDA are low for INT timeout time (0x9C[1:0].)

PD Power Mode - Idle Mode

Addr	Bit	BitName	Default	Type	Description
0x9B	3	**AUTOIDLE_EN**	0	RW	1 : Auto enter idle mode enable 0 : Auto enter idle mode disable
0x9B	2:0	**AUTOIDLE_TIMEOUT**	000	RW	Enter idle mode timeout time = (AUTOIDLE_TIMEOUT*2+1)*6.4ms

0x9B[3]=1b:
PD function will enter Idle mode automatically while PD_CCx does not communicate (receiving or transmission) for "Enter idel mode timeout time" (0x9B[2:0])
As PD_CCx communicates (receiving or transmission,) PD function will exit from idle mode automatically.

0x9B[3]=0b:
PD function will not enter Idle mode automatically while PD_CCx does not communicate (receiving or transmission) for "Enter idel mode timeout time" (0x9B[2:0])

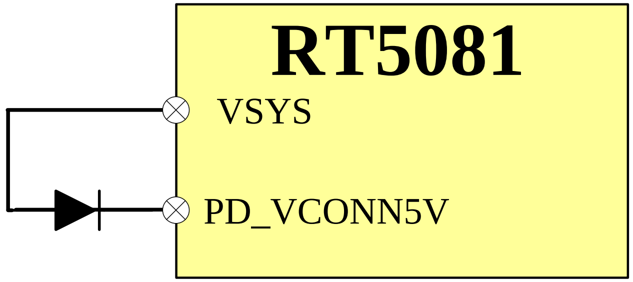
PD Power Mode – Shipping Mode

Addr	Bit	BitName	Default	Type	Description
0x9B	5	**SHIPPING_OFF**	0	RW	0: Shipping mode 1: Non-shipping mode

0x9B[5]=1b:
PD function will exit from shipping mode.

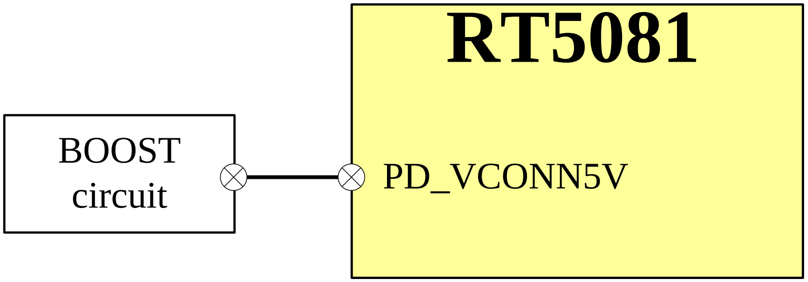
0x9B[5]=0b:
PD function will be in shipping mode after MT6370 power on.

Source selection for PD_VCONN5V



- **1.VSYS provides power to PD_VCONN5V**
  - Need to add diode between VSYS pin to PD_VCONN5V pin.
  - VCONN voltage range=3V-5.5V
  - We suggest below P/N for diode selection

Reference	Q'ty	P/N	Description	Package	Manufacturer
D6	1	NSR0320MW2T1G	SCHOTTKY DIODE	SOD- 323	On-semi



- **2.Another boost circuit provides power to PD_VCONN5V**
  - VCONN voltage range=3V-5.5V

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Content

- RT5081 Introduction
- General Function Description
- **Component Selection Guide**
- Schematic/Layout Notice

How to decide inductor SPEC of Charger

- IBAT target is 3A
- Low DCR to eliminate power loss, expect < 40m ohm
- Choose IDC2 (max) > Inductor current, expect > 3.9A
- For example :

Inductance [μH]	Tolerance (%)	Test Frequency (MHz)	Rdc Max(Typ) [mΩ]	Rated DC Current [A] Max(Typ)	
				ΔL/L=30% *1	ΔT=40[℃] *2
1.0	±20	1	40 (33)	4.7 (5.3)	3.3 (3.9)

Note: 1. The inductor current rating “must be” higher than Imax and inductance variation should be lower than +/-30% for all operation condition, included initial variation.

Note: 2. DCR value is suggested for efficiency for system and thermal performance, not must

How to decide inductor SPEC of Backlight

- Max ILX peak current <Inductor saturation current
- Low DCR to eliminate power loss.
- Choose saturation current higher than OVP level.

$$IL_{avg} = \frac{Vout * Iout}{Vin * eff} \qquad \Delta IL = \frac{Vin * Duty}{Freq * L} \qquad IL_{peak} = IL_{avg} + \frac{1}{2}\Delta IL$$

- For the 4p8s, Vin=3V, Iout=30mA/channel
- IL_{avg}=1.17A, ΔIL=0.266A, IL_{peak}=1.31A

Example:MDMK4040T100MM

Nominal Inductance [uH]	Inductance Tolerance [%]	DC Resistance [mΩ]	Inductance Decrease Current IDC1 (A) (typ.)	Temperature Rise Current IDC2 (A) (typ.)
10	+/-20	280	2	1.6

- I_{DC1}: DC current (A) that will cause L_0 to drop approximately 30%
- I_{DC2}: DC current (A) that will cause an approximately Δ40 degC
- DCR value is suggested for efficiency and system thermal performance; not a must.

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How to decide inductor SPEC of Display Bias

- DB BOOST OCP target is 1.32A
- Low DCR to eliminate power loss, expect <90mΩ
- Choose IDC2(max)>$I_{inductor(max)}$ current, expect >1.32A

$$IL_{avg} = \frac{Vout * Iout}{Vin * eff} \qquad \Delta IL = \frac{Vin * Duty}{Freq * L} \qquad IL_{peak} = IL_{avg} + \frac{1}{2}\Delta IL$$

- For the VBST=6.2V, Vin=3V, IPOS=INEG=150mA
- IL_{avg}=0.69A, ΔIL=0.704A, IL_{peak}=1.04A

Example.DFE252012R-H-2R2M

Nominal Inductance [uH]	Inductance Tolerance [%]	DC Resistance [mΩ]	Inductance Decrease Current IDC1 (A) (typ.)	Temperature Rise Current IDC2 (A) (typ.)
2.2	+/-20	75	3	2.4

- I_{DC1}: DC current (A) that will cause L_0 to drop approximately 30%
- I_{DC2}: DC current (A) that will cause an approximately Δ40 degC
- DCR value is suggested for efficiency and system thermal performance; not a must.

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- RT5081 Introduction
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- **Schematic/Layout Notice**

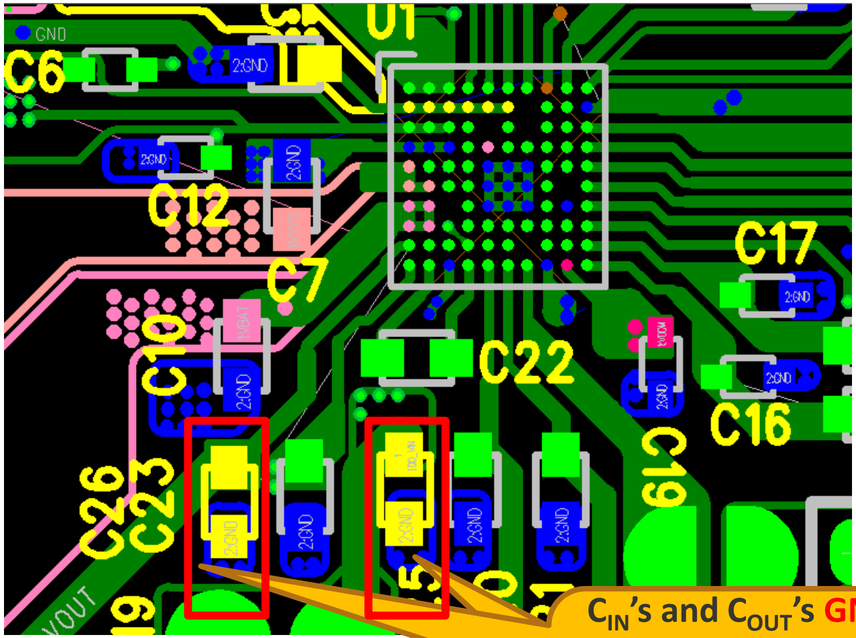
Schematic/Layout Notice

- High current path must enlarge trace width as 25mil/1A.
  - CHG_VIN, CHG_VLX, CHG_VMID, FL_VMID, VSYS and VBAT
- Bypass CAP/Resistor near to related ball.
  - VDDM, VDDA, BL_VDDA, DB_VDDA, CHG_BOOT to CHG_VLX, and CHG_ILIM.
- Inductor close to LX pins.
- VDDM and VDDA, BL_VDDA and DB_VDDA cap's GND should be directly connected to GND plane.

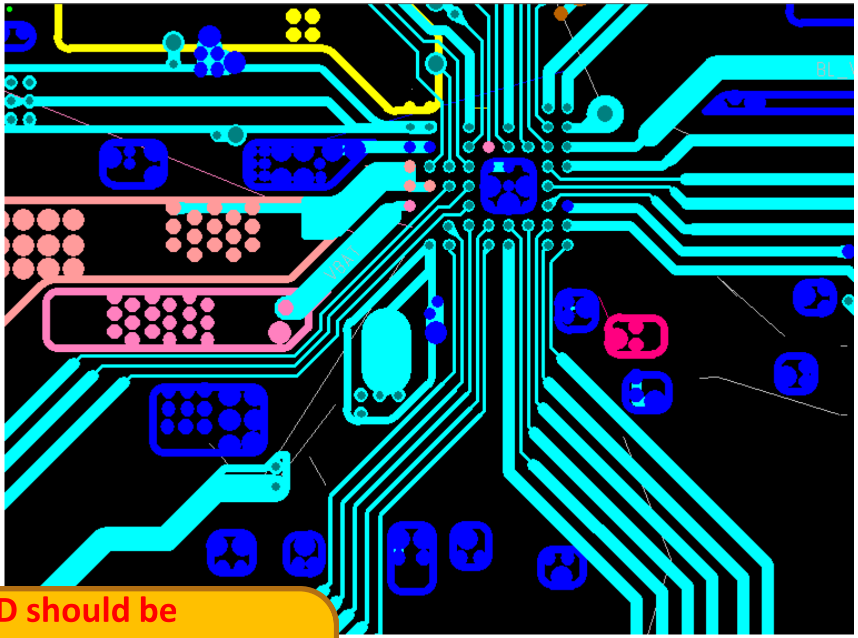
PCB Notice: LDO part

- Place CIN / COUT as close to LDO_VIN / LDO_VOUT pin as possible.
- CIN's and COUT's GND **should be isolated on the top layer** and then connect the pad of the capacitor directly with vias to the main ground plane.

Top Layer



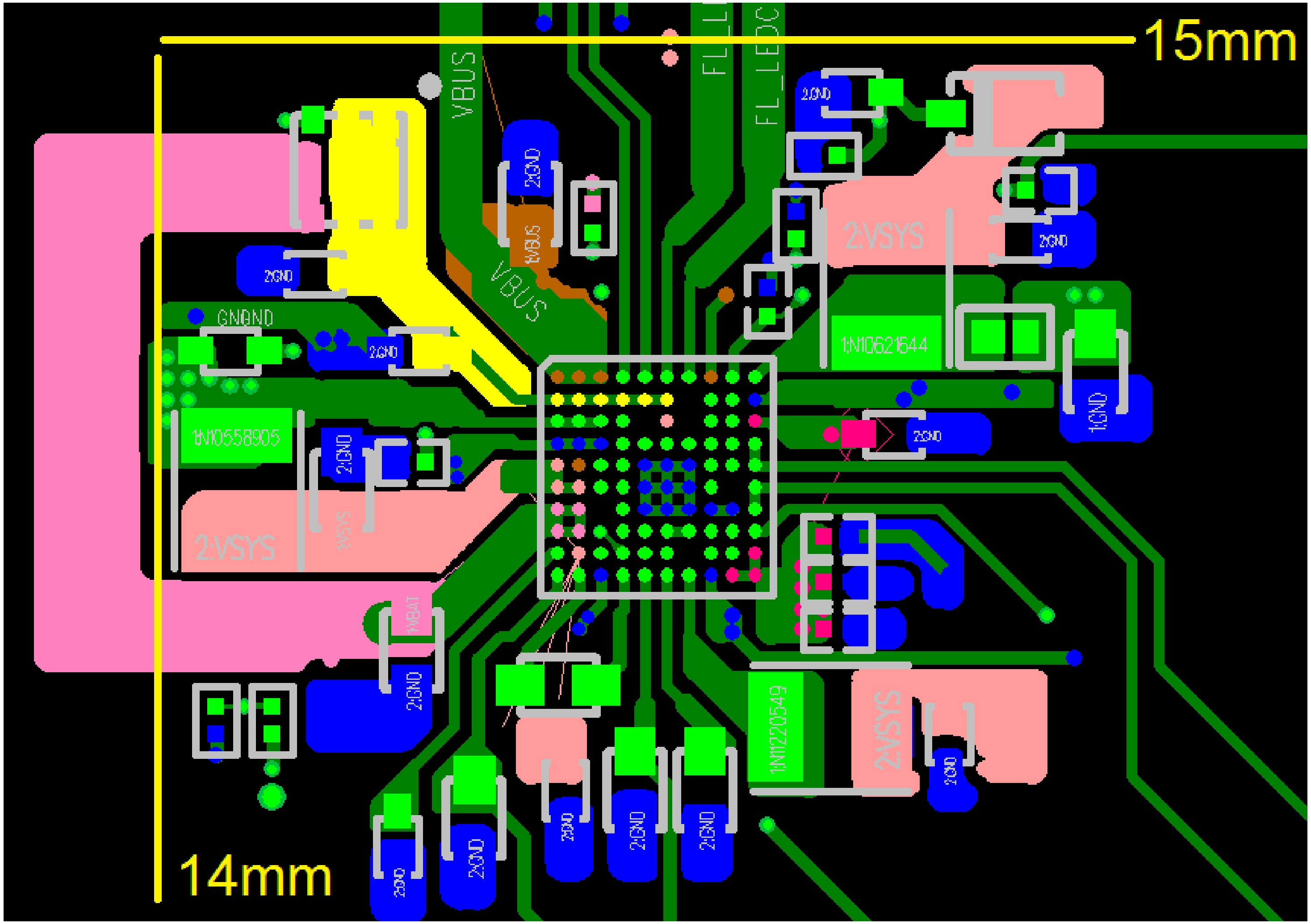
Layer 2



C_{IN}'s and C_{OUT}'s **GND should be isolated on the top layer** and then connect the pad of the capacitor directly with vias to the main ground plane.

Minimum PCB placement area requirement

By HDI-1 PCB stack rule, the minimum PCB placement area is 15mm x 14mm for support fully function



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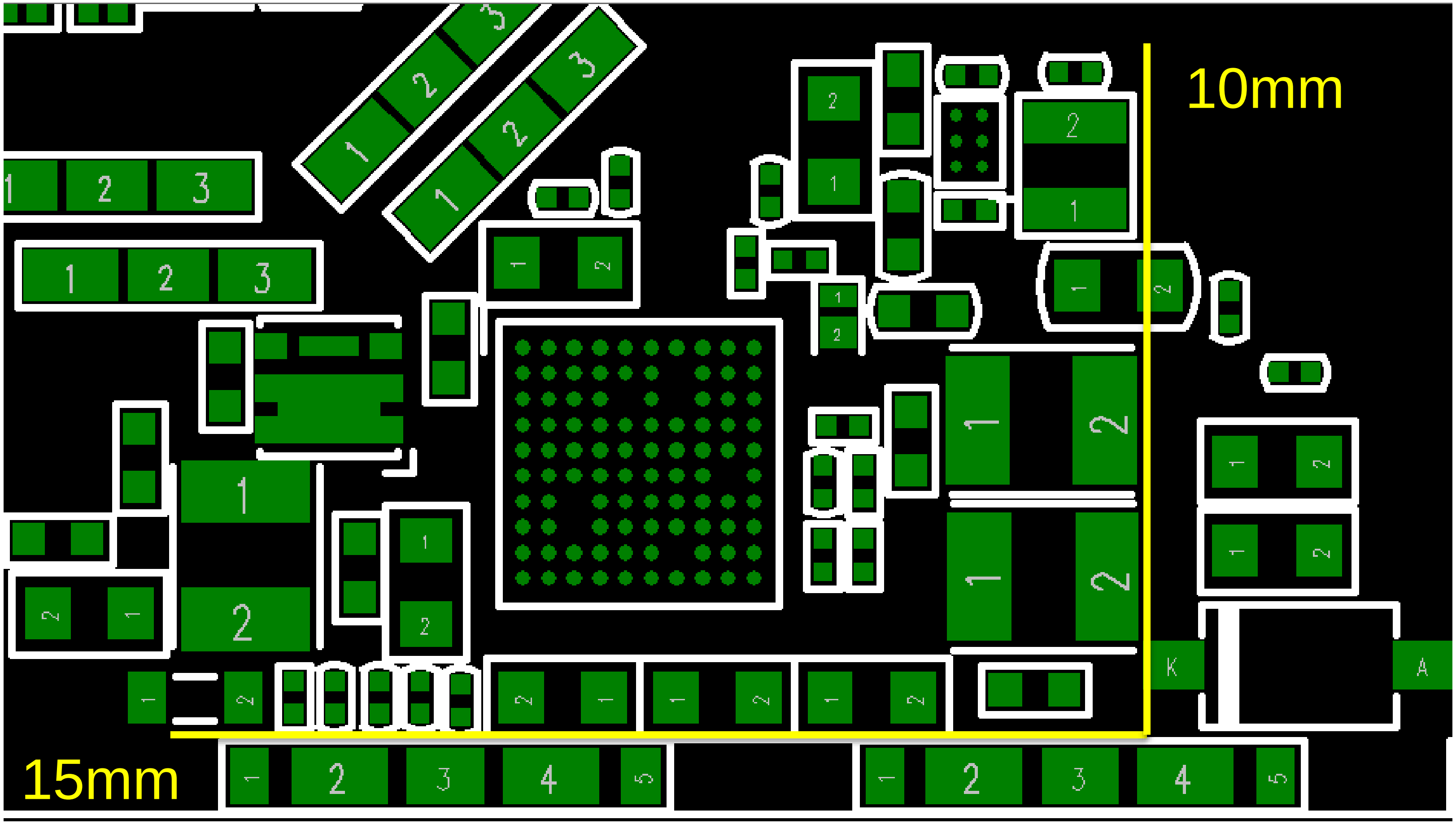
Minimum PCB placement area requirement

By HDI-2 PCB stack rule, the minimum PCB placement area is 15mm x 10mm for support fully function



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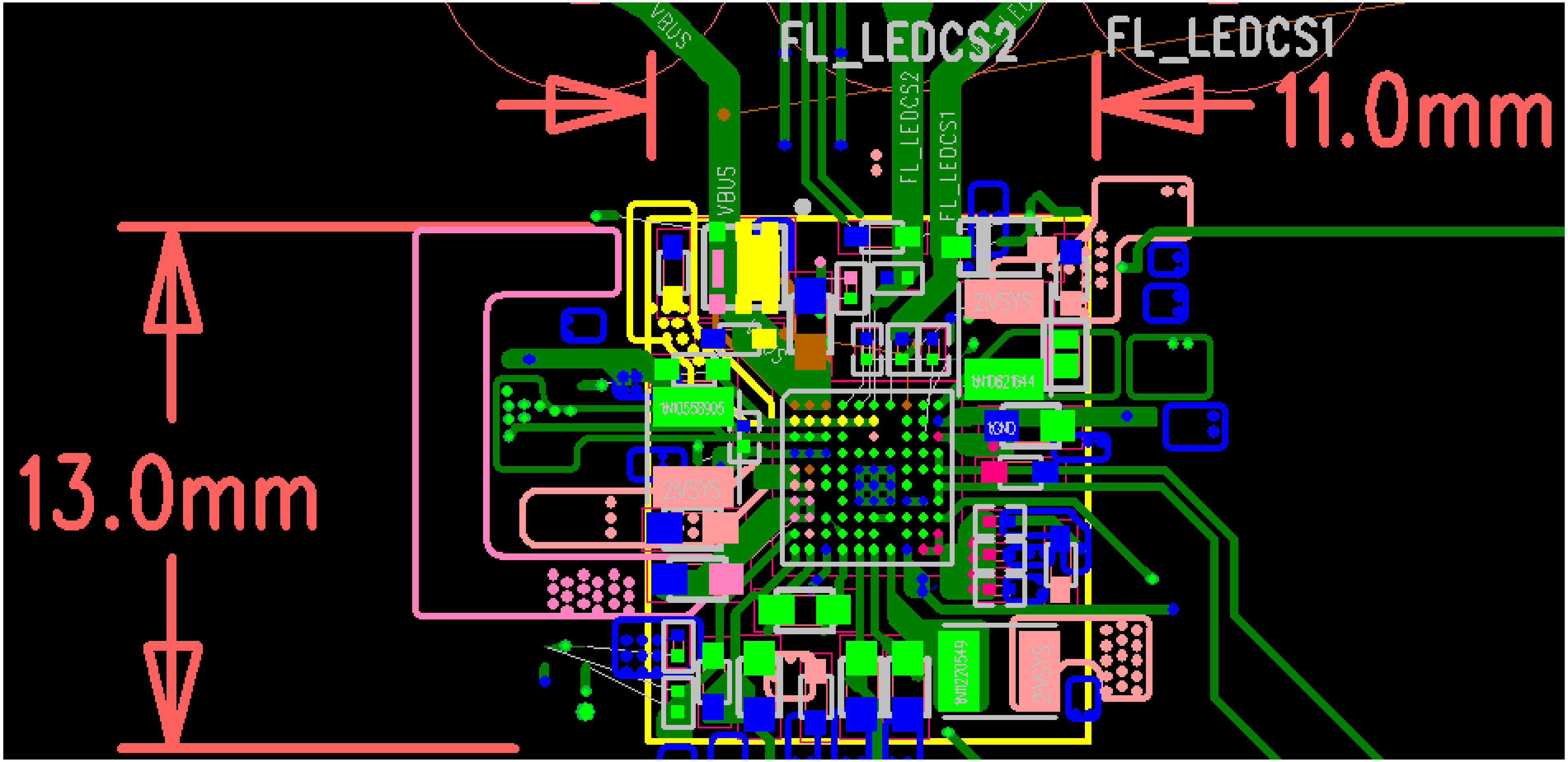
Minimum PCB placement area requirement

By HDI-3 PCB stack rule, the minimum PCB placement area is 13mm x 11mm for support fully function



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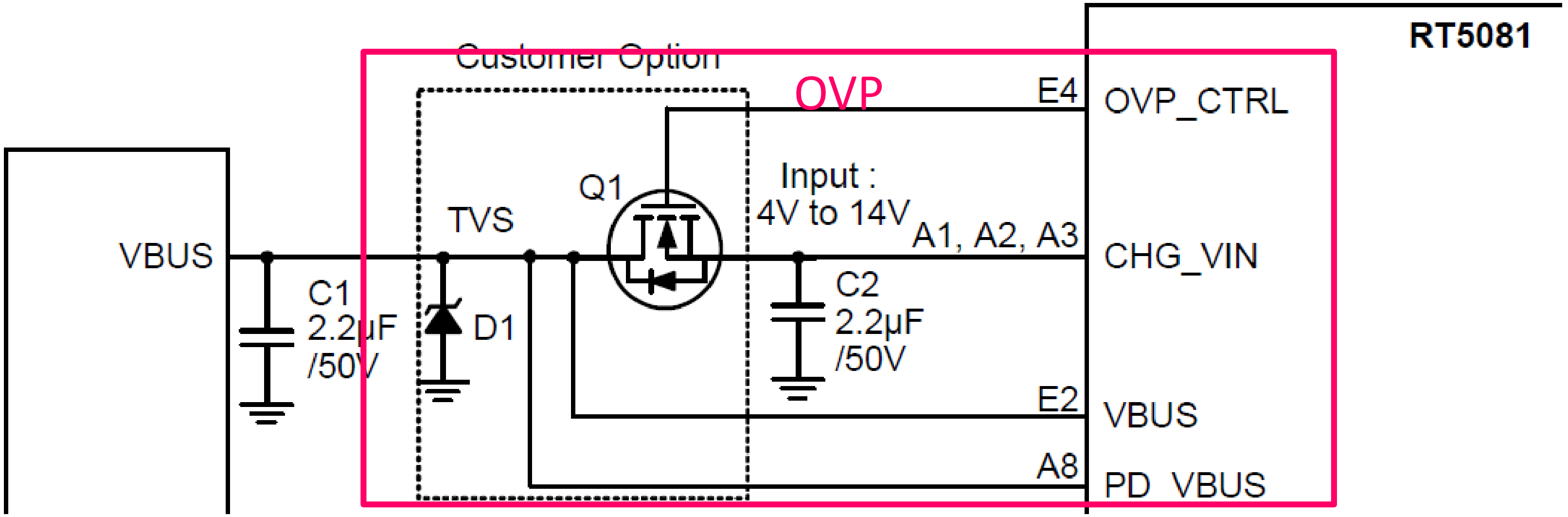
Option function: External OVP MOS controller



- OVP Controller
  - VBUS AMR up to 28V is higher than CHG_VIN AMR=22V
  - Over-Voltage Protection Threshold 16.5V is higher than $V_{BUS_OVP_CHG}$=14.5V
  - Over-Voltage Protection Hysteresis 200mV
  - OVP Propagation Delay for MOS turn off 0.18us for surge immunity
  - OVP Recovery Delay 8ms
  - The OTG Soft Start time around 30ms with external OVP MOS
  - The recommend external MOSFET is shown below:

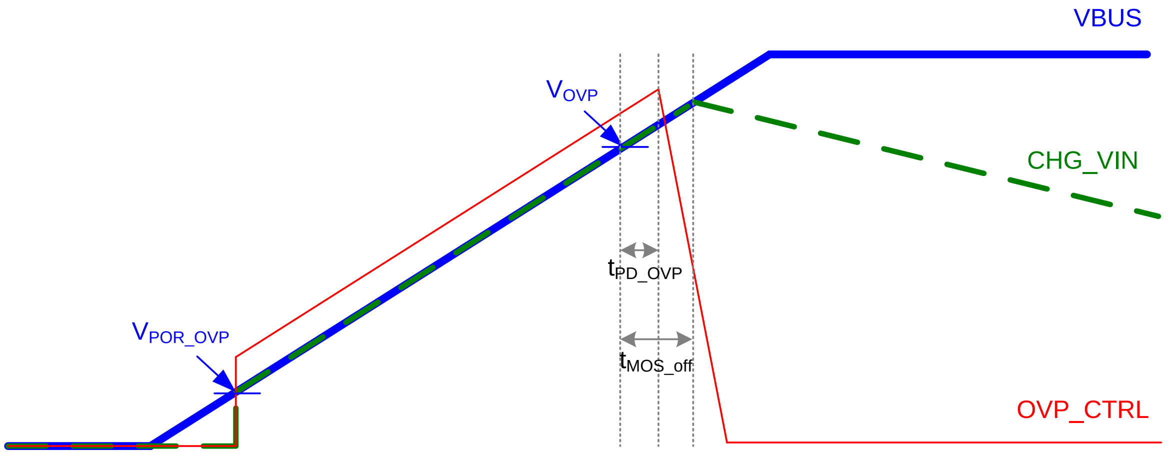
Reference	Q'ty	P/N	Description	Package	Manufacturer
Q1	1	DMN3016LFDF	N-Channel 30 V VGS+/-20V MOSFET	DFN 2x2	DIODES

OVP Controller Specification

- RT5081 define the propagation delay(t_{PD_OVP}) from the VBUS>VOVP to OVP_CTRL start falling.
- The delay time from the VBUS>VOVP to CHG_Vin start falling as following table

Note: Q1 MOS: DMN3016LFDF
Ceq of CHG_VIN: 2.2uF

RT5081_EVB_V1	t_{PD_OVP}	t_{MOS_off}
5 to 20V in 8us	180ns	250ns
12 to 20V in 8us	180ns	250ns



Surge Protection → TVS selection

- Follow IEC 61000-4-5 standard. We suggest the below TVS diodes for surge protection.

P/N	Ipp	VBR	Description	Package	Manufacturer
ESD5641D12	150A	15V	For Surge=300V from VBUS	DFN2x2_3L	Will Semi
PTVSHC3N12VU	200A	14.5V	For Surge=450V from VBUS	DFN2x2_3L	Prisemi
PTVSHC3D4V5B	130A	4.5V	For Surge=300V from VBAT	SOD-323	Prisemi

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OVP Type Comparison

TYPE	Protection method	Recover method
W/o Ext. MOS Q1 (Internal OVP)	CHG_VIN pin>14.5V, charger shutdown CHG_VIN pin AMR =22V (VBUS=CHG_VIN)	CHG_VIN <14.25V
With Ext. MOS Q1 (OVP controller)	VBUS pin>16.5V, turn off Q1 VBUS pin AMR =28V (VBUS≠CHG_VIN)	VBUS pin <16.3V
OVP IC (FPF2281)	VBUS>14V, turn off MOS	VBUS <13V

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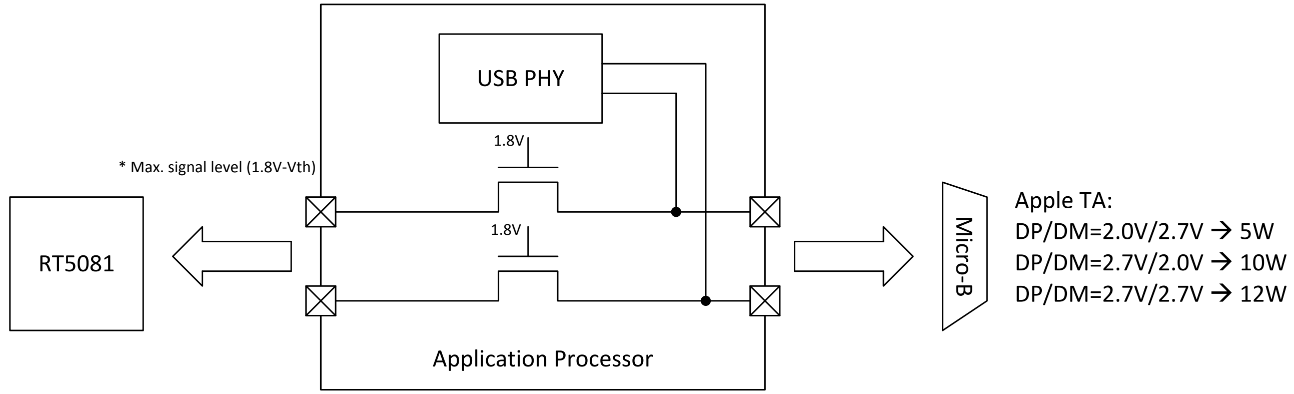
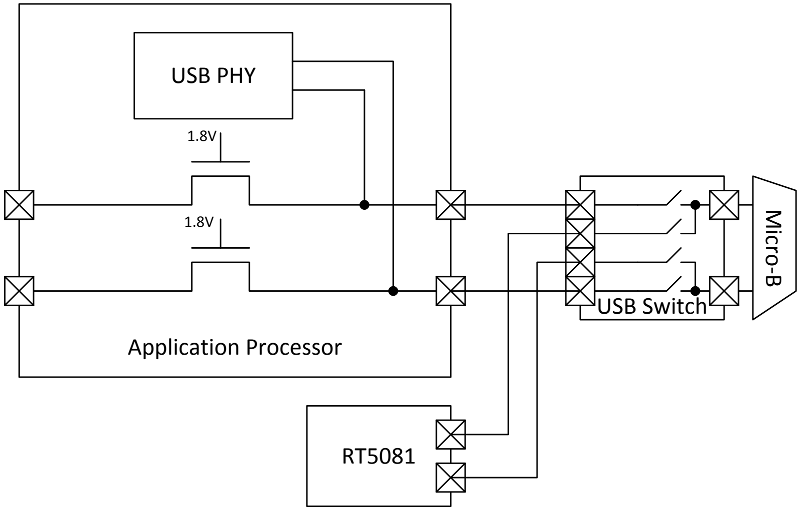
Option function: Apple TA Detection

- AP NMOS switch can’t pass 2.0V/2.7V from Apple TA.
- External USB switch is needed to overcome this issue.



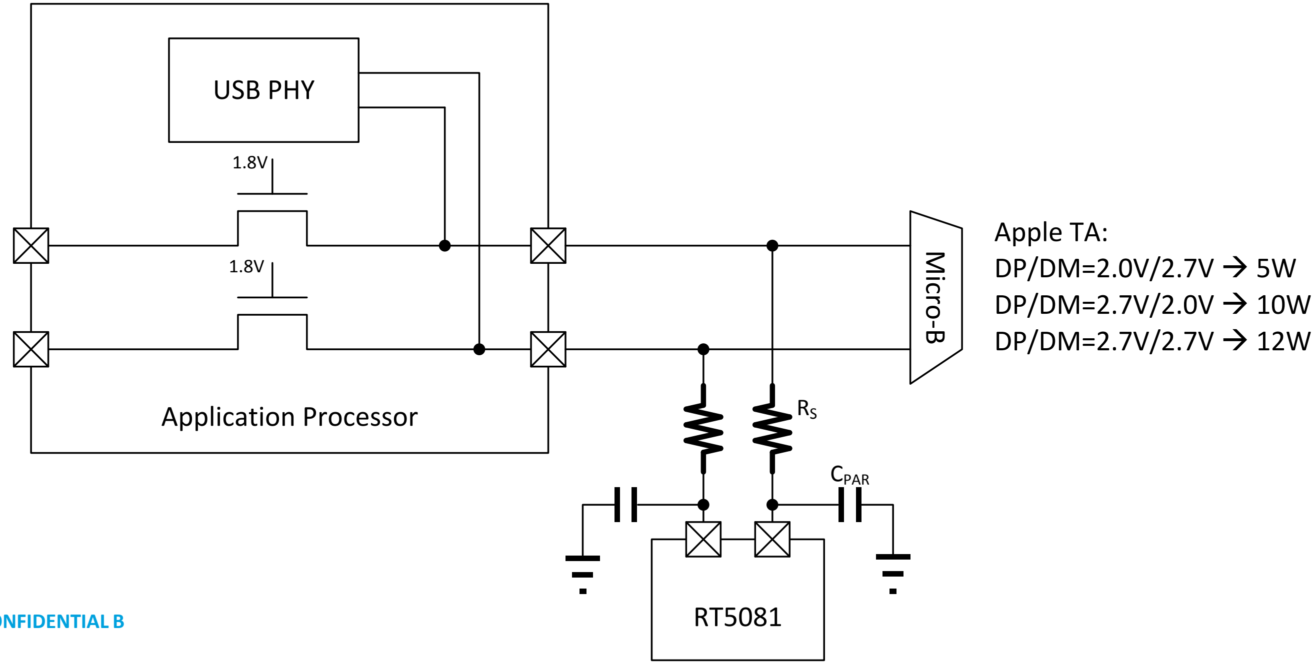


Option function: Apple TA Detection

- DP/DM of RT5081 connects Micro-B directly by well-defined PCB. (R_S and C_{PAR})
  - Need to do impedance matching.

→Guarantee USB eye diagram performance.

→Guarantee BC1.2 detection works normally.



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